長 龍 國 際

先進的半導體
3D封裝專利技術

- 全球半導體與記憶體
- 中國的記憶體產業增長
- 2D 到 3D NAND 需求向上提升
- 記憶體封裝技術
- 長龍國際半導體3D封裝技術

全球半導體和記憶體市場

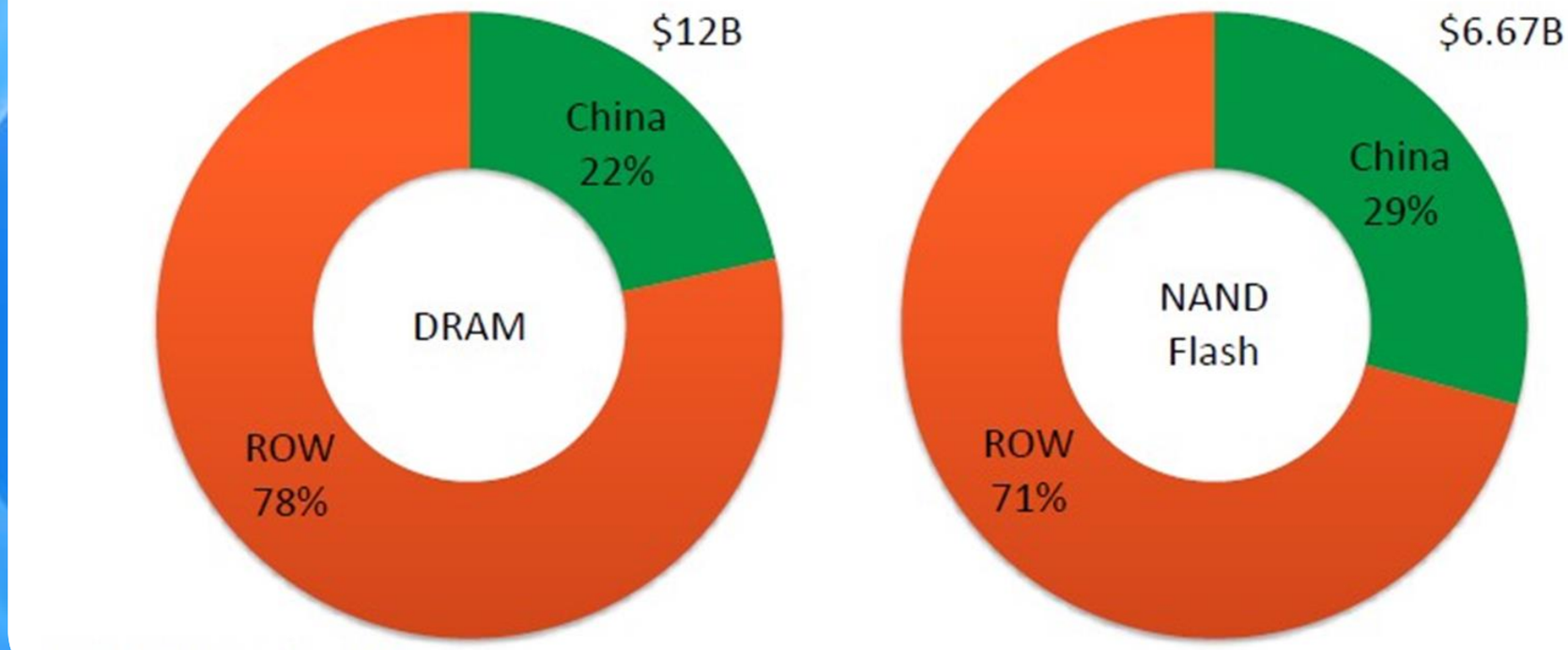
記憶體佔全球半導體四分之一的產量

數據存取需求爆炸性的成長

1 ZB = 10^{21} bytes = 1000,000,000,000 GB

大數據顯示“移動/計算應用中的廣泛部署而正在創建。
數據是未來十年的新“石油”。

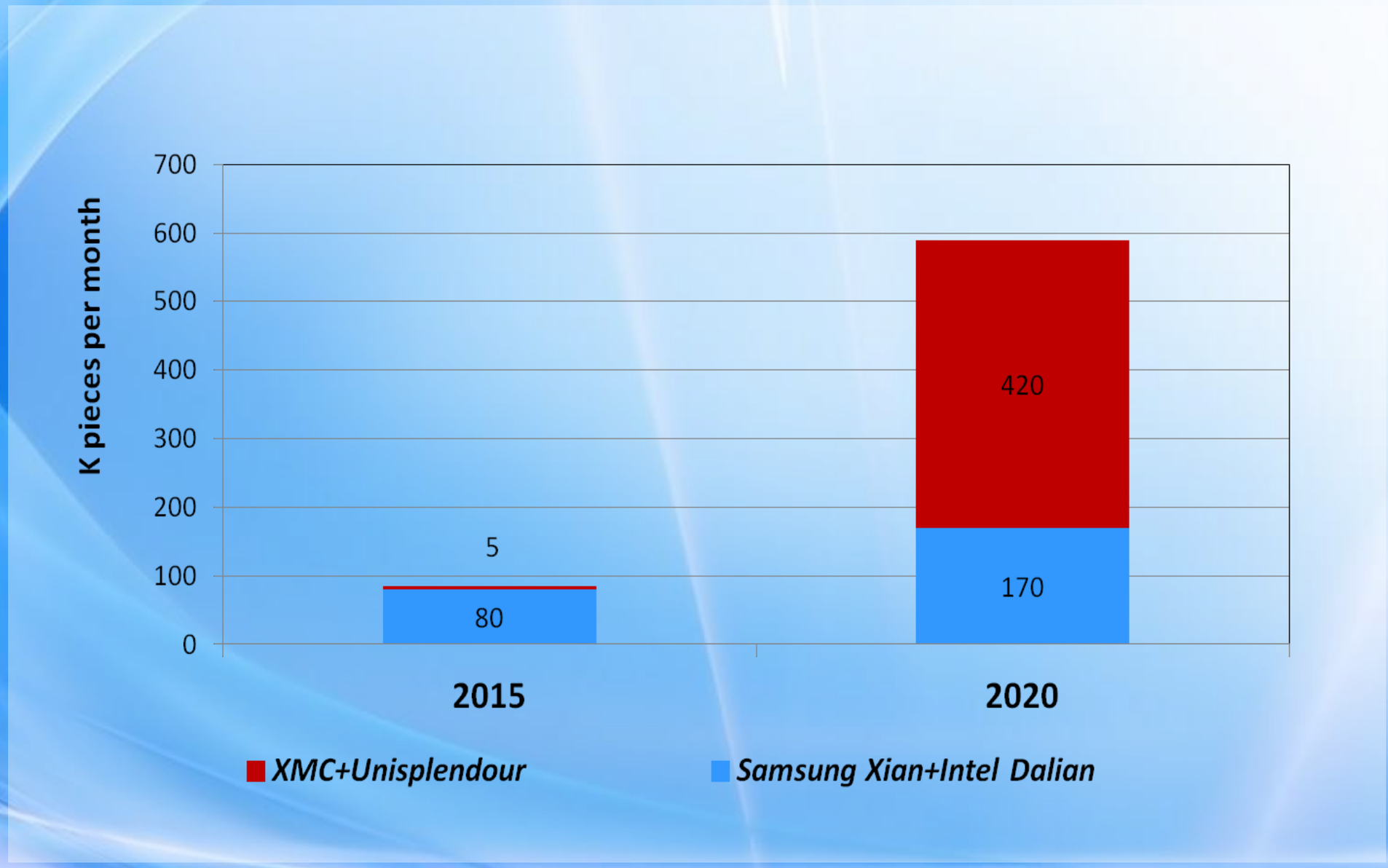
中國的記憶體需求



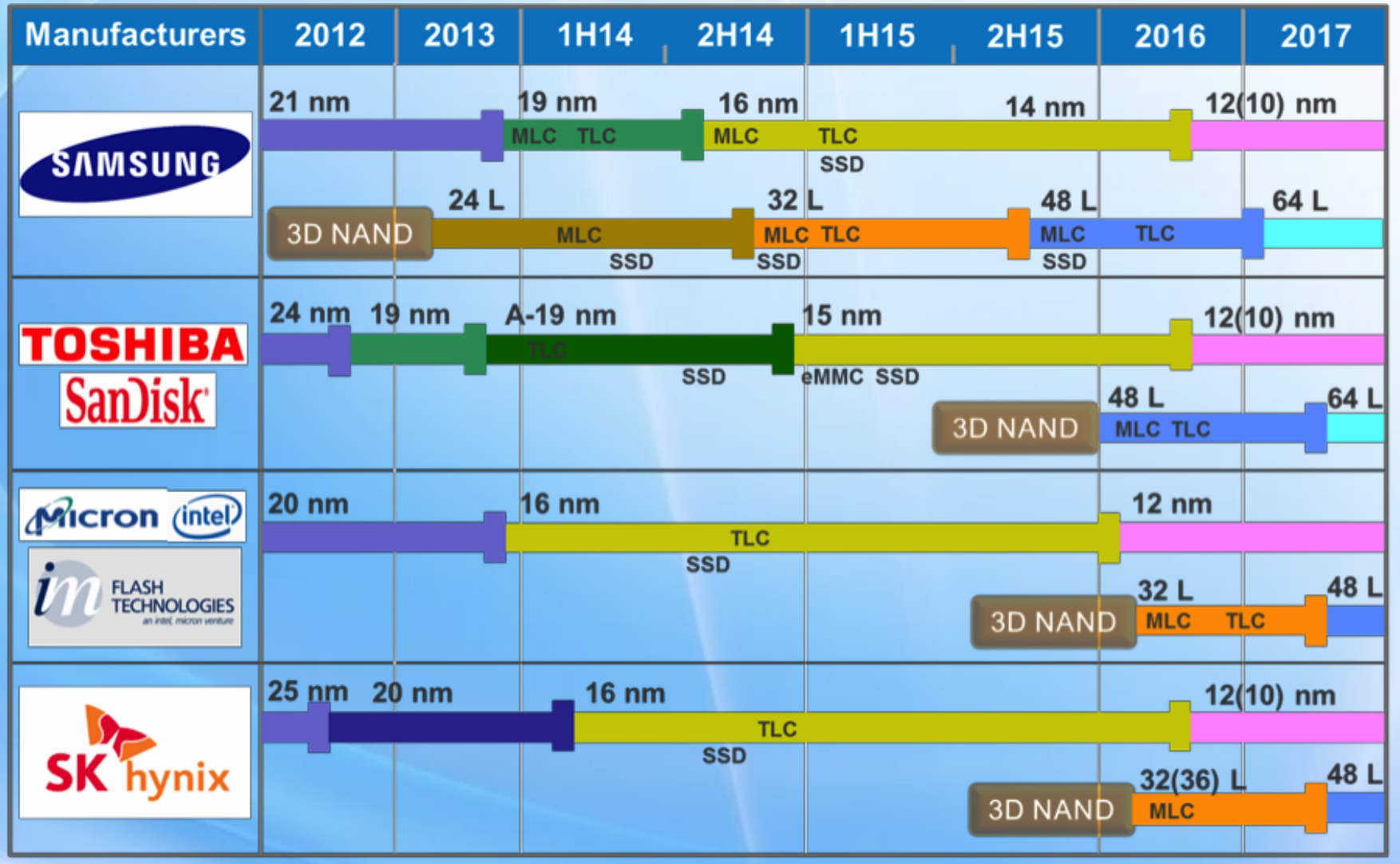
Source: TrendForce, Oct., 2015

隨著PC智能手機的興起，中國國內DRAM和NAND閃存消費量急劇增加。 中國占世界記憶產量的30%左右，其中大部分都是由國外進口製造。

NAND Flash需求



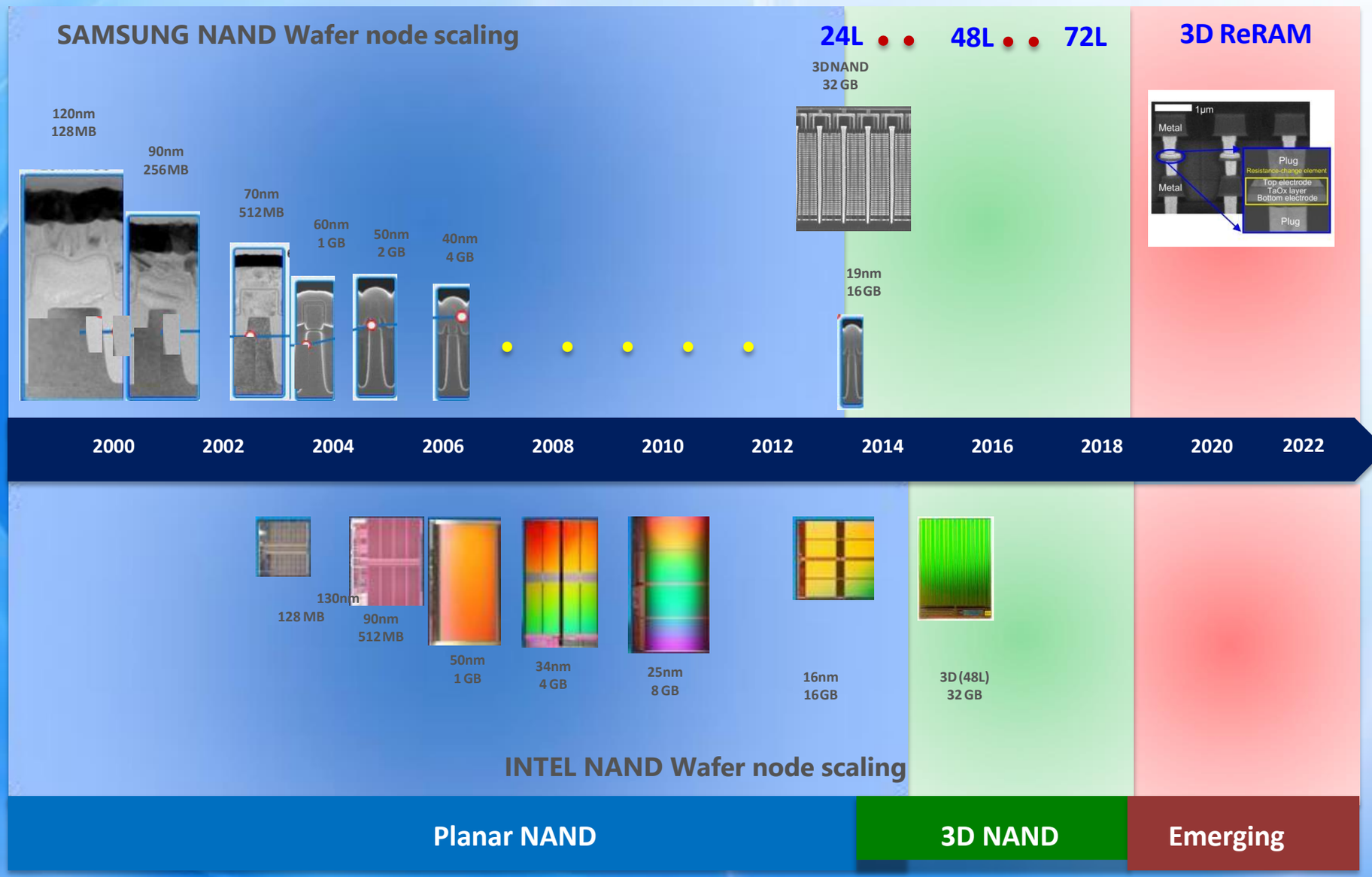
各廠3D封裝技術進程


Manufacturers
2012
2013
1H14
2H14
1H15
2H15
2016
2017
SAMSUNG
21 nm
19 nm
16 nm
14 nm
12(10) nm
MLC TLC
MLC
TLC
SSD
3D NAND
24 L
32 L
48 L
64 L
MLC
SSD
MLC TLC
SSD
MLC
TLC
SSD
TOSHIBA
SanDisk
24 nm
19 nm
A-19 nm
15 nm
12(10) nm
TLC
SSD
eMMC SSD
3D NAND
48 L
64 L
MLC TLC
Micron
intel
FLASH TECHNOLOGIES
20 nm
16 nm
12 nm
TLC
SSD
3D NAND
32 L
48 L
MLC
TLC
SK hynix
25 nm
20 nm
16 nm
12(10) nm
TLC
SSD
3D NAND
32(36) L
48 L
MLC

全球半導體中心的戰略圖

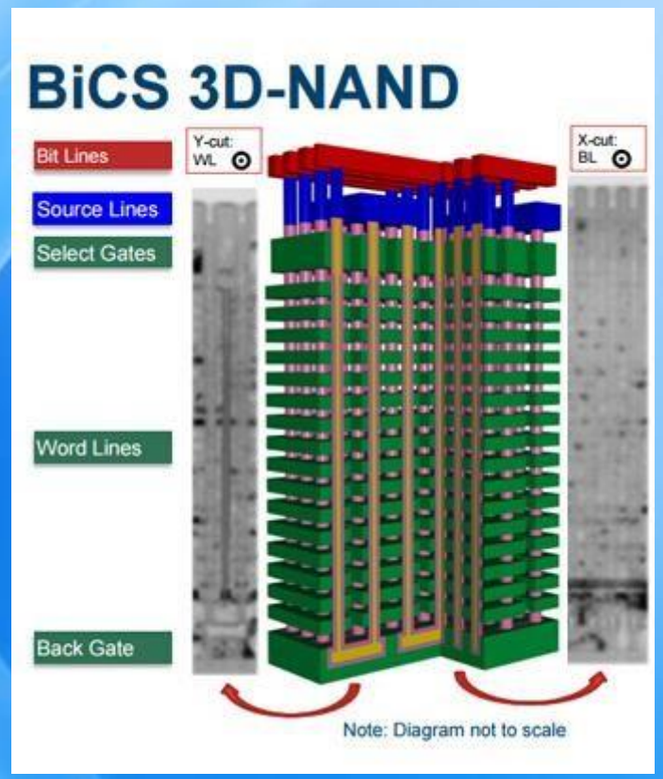
Zoom in on China factory locations

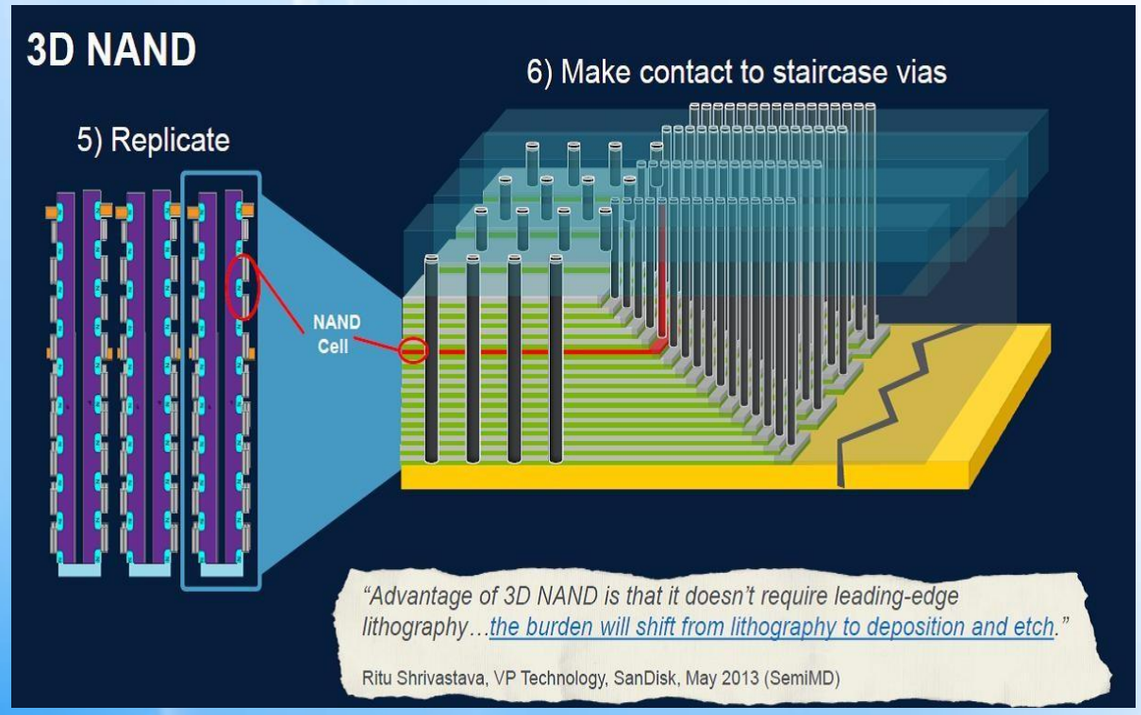
3D NAND發展進程

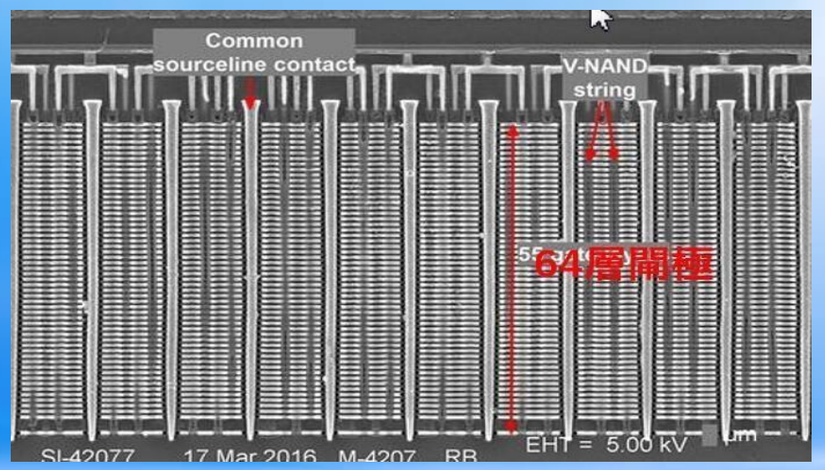


3D NAND技術提供的擴展經濟效益顯著降低了

3D封裝技術概念圖


BiCS 3D-NAND
Bit Lines
Source Lines
Select Gates
Word Lines
Back Gate
Y-cut: WL
X-cut: BL
Note: Diagram not to scale

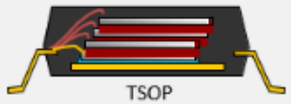

3D NAND
5) Replicate
6) Make contact to staircase vias
NAND Cell
"Advantage of 3D NAND is that it doesn't require leading-edge lithography…the burden will shift from lithography to deposition and etch."
Ritu Shrivastava, VP Technology, SanDisk, May 2013 (SemiMD)


Common sourceline contact
V-NAND string
64層開極
SI-42077 17 Mar 2016 M-4207 RB
EHT = 5.00 kV

3D封裝技術應用範圍

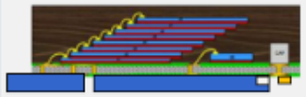
各種堆疊方式應用範圍

REMOVABLE



TSOP

SD -SiP



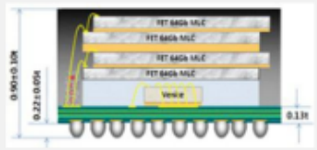
USB-SiP

MicroSD

MOBILE / WEARABLE

Single chip eWLB

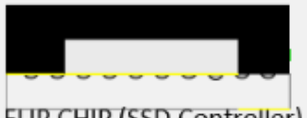
UFS



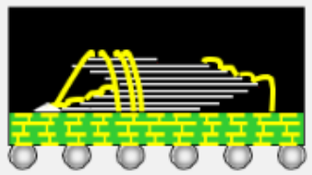
eMMC

eMCP

CLIENT SSD

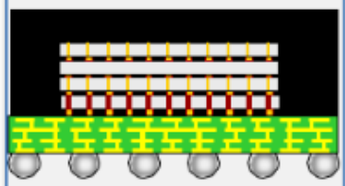


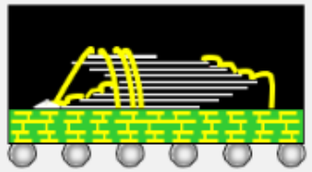
FLIP CHIP (SSD Controller)



FBGA-SD

ENTERPRISE SSD





FBGA-SD

AUTOMOTIVE

SD -SiP

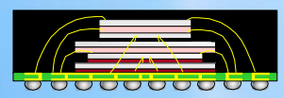
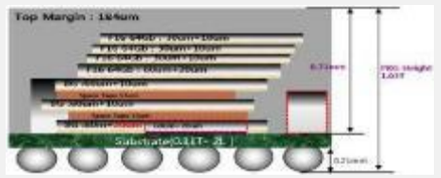
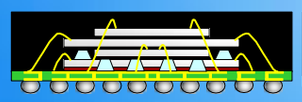
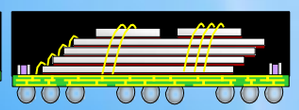
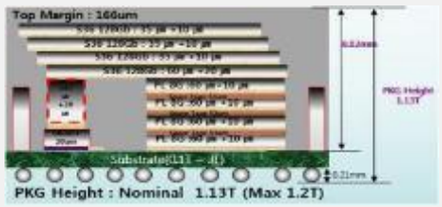
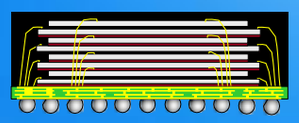
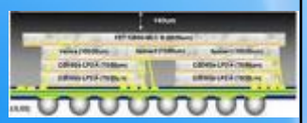
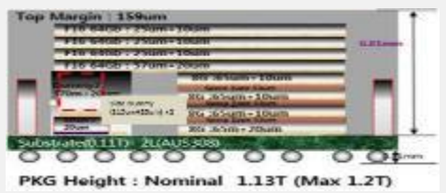
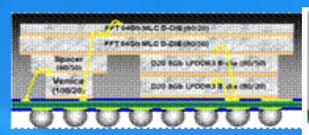
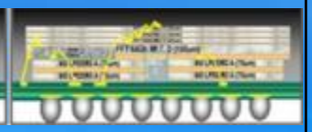
TSOP

MicroSD

記憶替封裝趨勢

目前技術 → 趨勢

HVM

PoP	FBGA	LGA	
FBGA-PoPt-SD2(2D) 	FBGA-SD4(4D+3W)  FBGA-SD5(5D+2W) 	Micro SD 4+1 SD SiP 	 TFBGA-SD7, 30 um WT, 1.03mm PGK T
FBGA-PoPt-SD3(3D+2W) 	FBGA-SD4(4D+0W)  FBGA-SD6, eMMC 	Dual Driver USB 8+1 	 TFBGA-SD8, 35 um WT, 1.13mm PGK T
FBGA-PoPt-SD4(4D+1W) 	FBGA-SD8(8D+0W)  VFBGA-SiP-SD8 	SD-SiP 	 TFBGA-SD8, 25 um WT, 1.13mm PGK T
FBGA-PoPt-SD4 	VFBGA-MD6  VFBGA-MD7 		
WFBGA-PoPt-SD4 	VFBGA-SiP-SD8  VFBGA-SiP-SD9 		 XL/MC-eWLB

L=1.4mm, T=1.2mm, V=1.0mm, W=0.8mm, U=0.65mm, X=0.50mm

LFBGA-SD8 (NAND)

Package Features

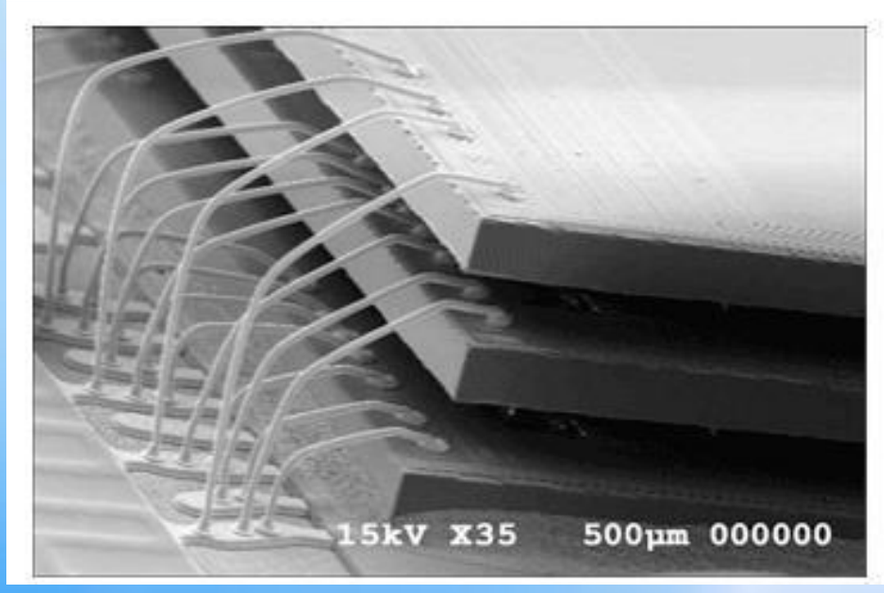
- LFBGA 14x18mm 152LD
- NAND Die Size : 9.7x17.1mm
- Device : 20nm Non-LowK NAND
- Wafer thickness : 60um
- Mold cap: 0.84mm
- 2-lyr / 0.13mmT laminate substrate

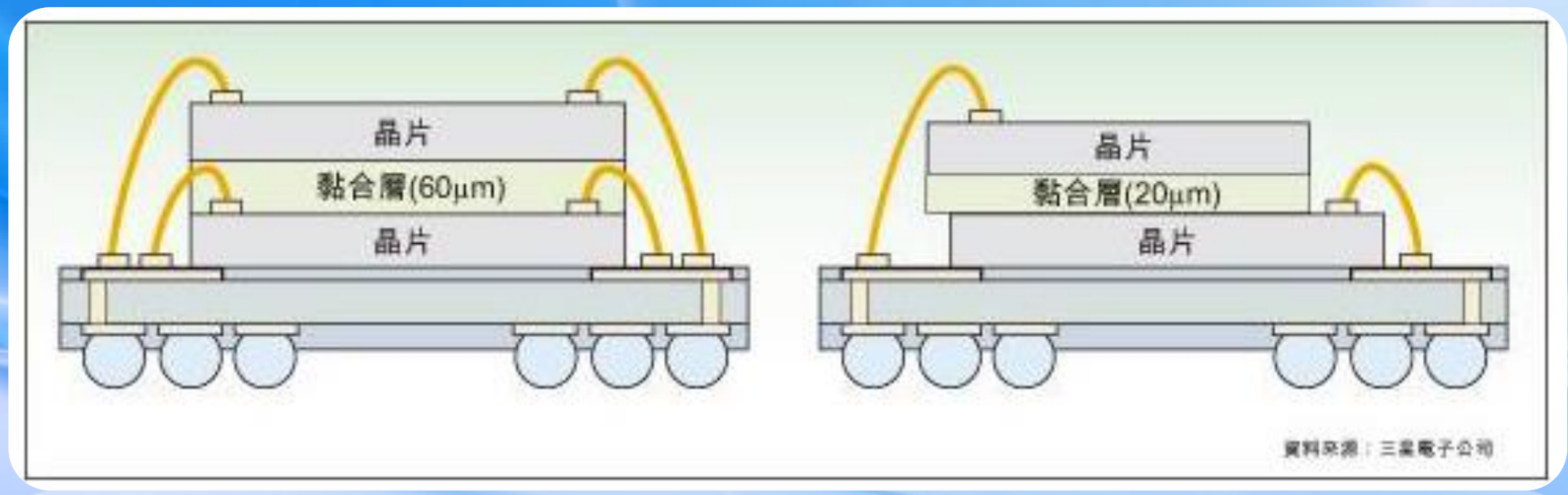
Key Technologies

- 20nm NAND die
- 0.5mm overhang W/B with 60um die thickness
- 2-passes DA for the 8 dies stack

Current Status

- **HVM since 2011**





記憶體堆疊晶片封裝– MIXED (FBGA-SD6)
NAND + DDR + CONTROLLER

Package Features

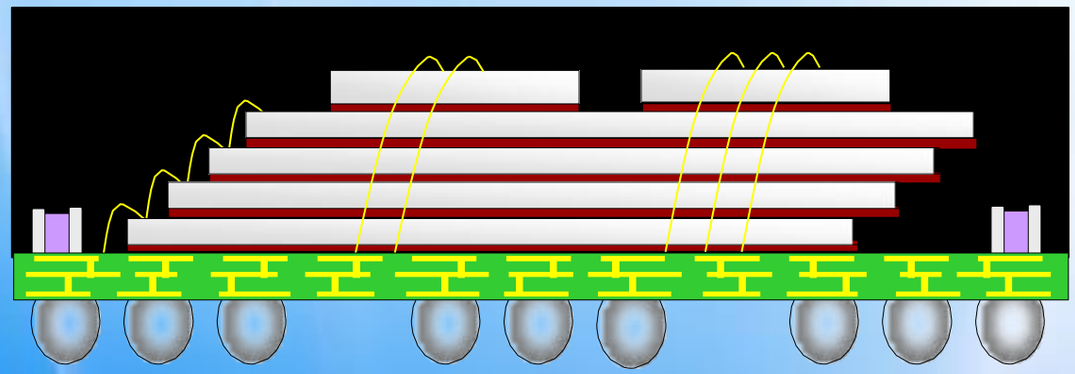
- VFBGA-SD6 11.5x13mm 153LD
- Nand flash Die Size: 10.33x8.12mm
- DDR Die Size: 6.32x2.69mm
- Controller Die Size: 6.79X1.82mm
- 0.13mm, 3-lyr coreless substrate

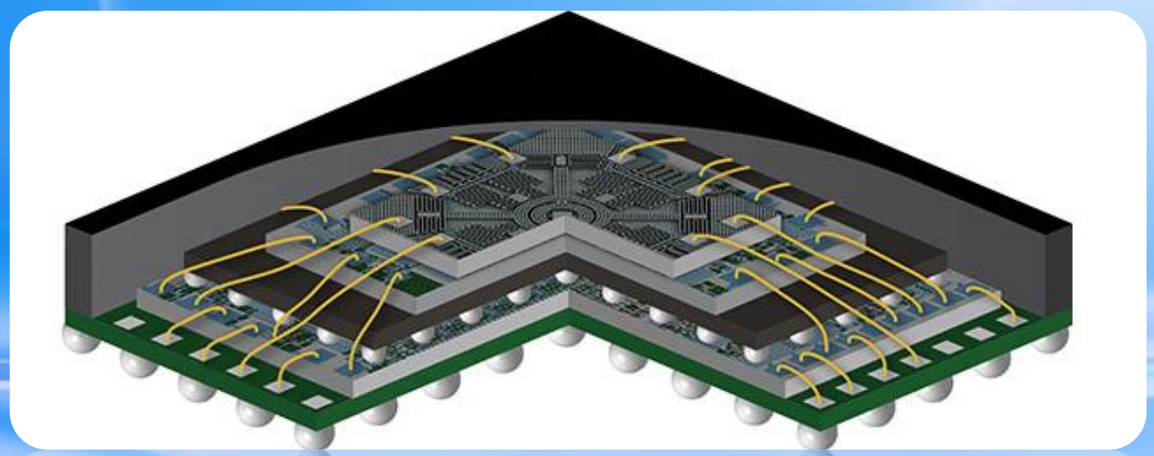
Key Technologies

- 0.13T odd layer substrate handing
- SSB loop for die to die and die to substrate
- Warpage control w/ 3L substrate

Current Status

- **HVM since 2012**





FLGA-SD9 (USB)

Package Features

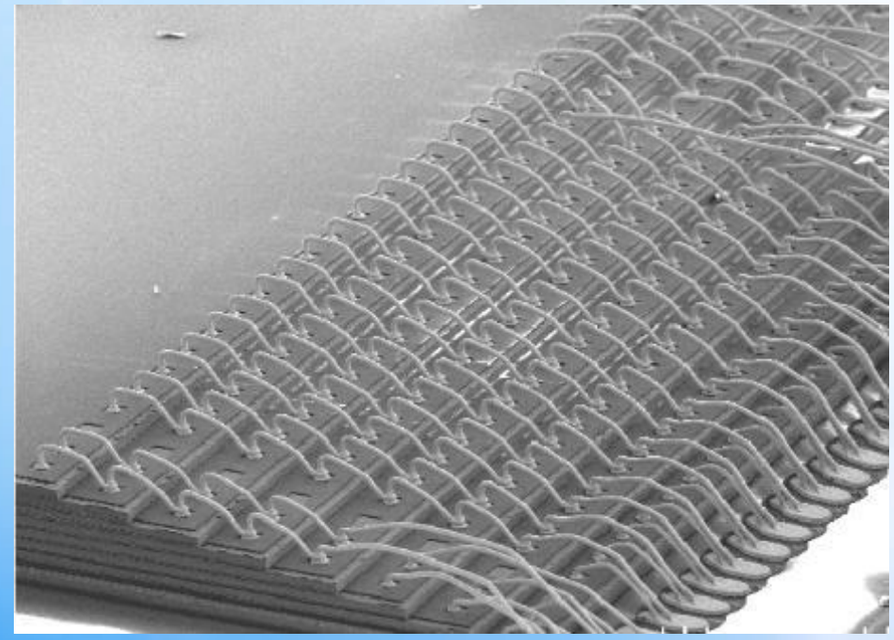
- FLGA 11.1x16mm
- Memory Die Size : 8.2x11.1mm
- Controller Die Size: 2.9x2.4mm
- Device : 19nm Non-LowK + 65nm Lowk Controller
- Wafer thickness : 68um x 8 dies + 150um Controller
- 2-lyr / 0.21mmT laminate substrate

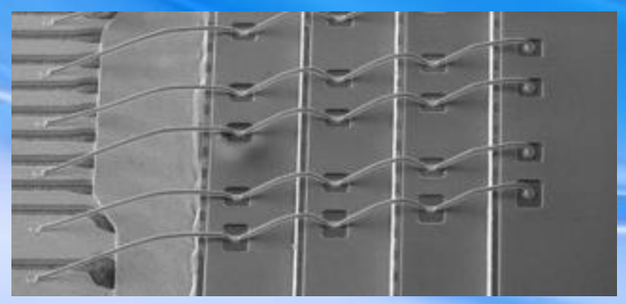
Key Technologies

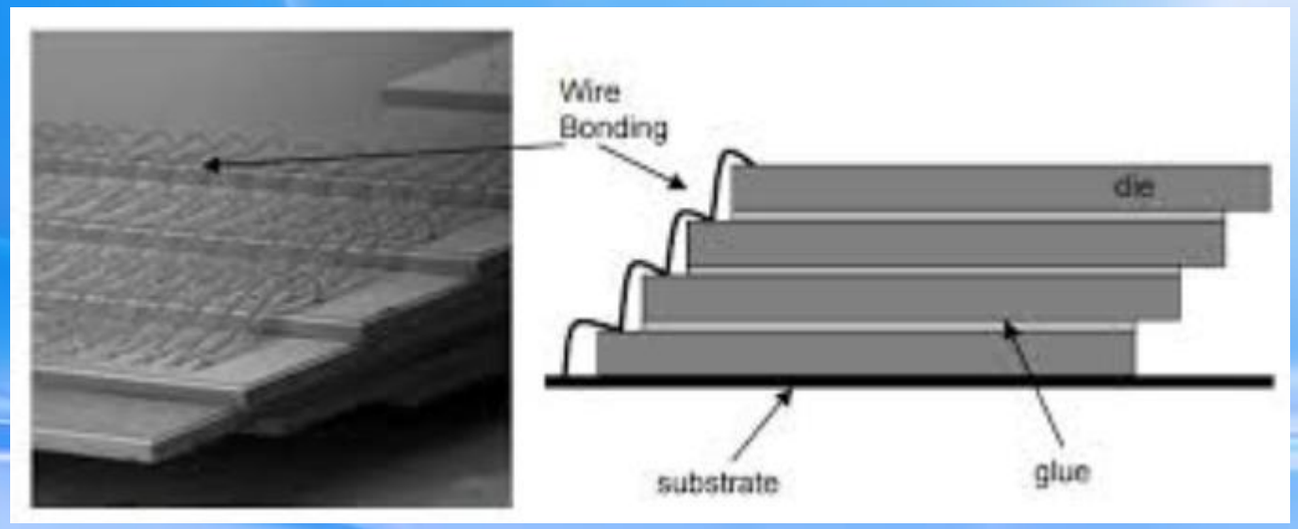
- 19nm NAND die
- 8-Die Stack with Die-to-die bonding
- One-pass for the 8 NAND dies stack

Current Status

- **HVM**







Memory Stacked-Die

Package Features

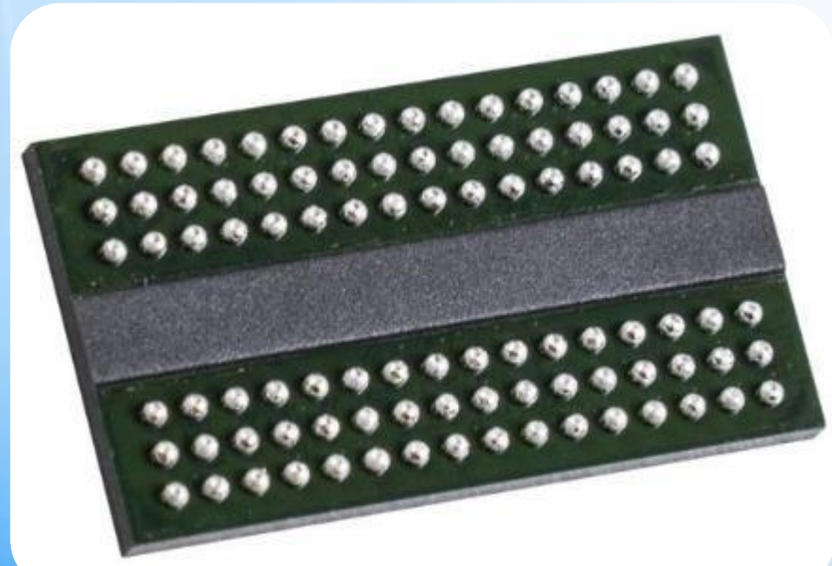
- FBGA 11.5x13mm 221LD e-MCP
- 4.115x1.385(Controller) : 60um
- 9.647x8.070(DRAM) : 75um
- 1.208x7.171(Nand) : 60um
- 9.00x8.00 (Film spacer) : 53um
- 2-lyr / 0.41mmT laminate substrate

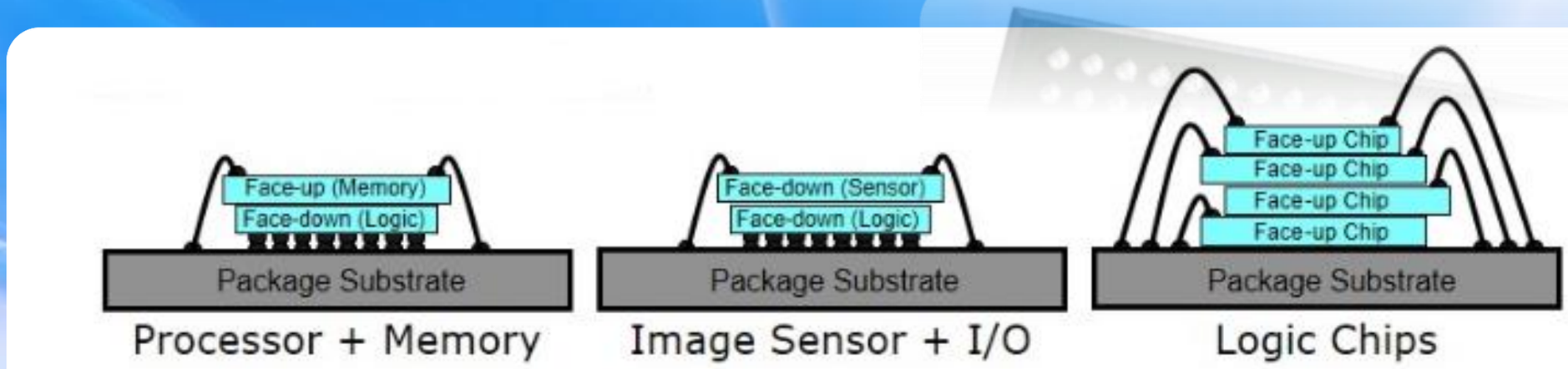
Key Technologies

- 60um NAND flash die
- Film spacer application
- Dolmen and NAND cascade structure

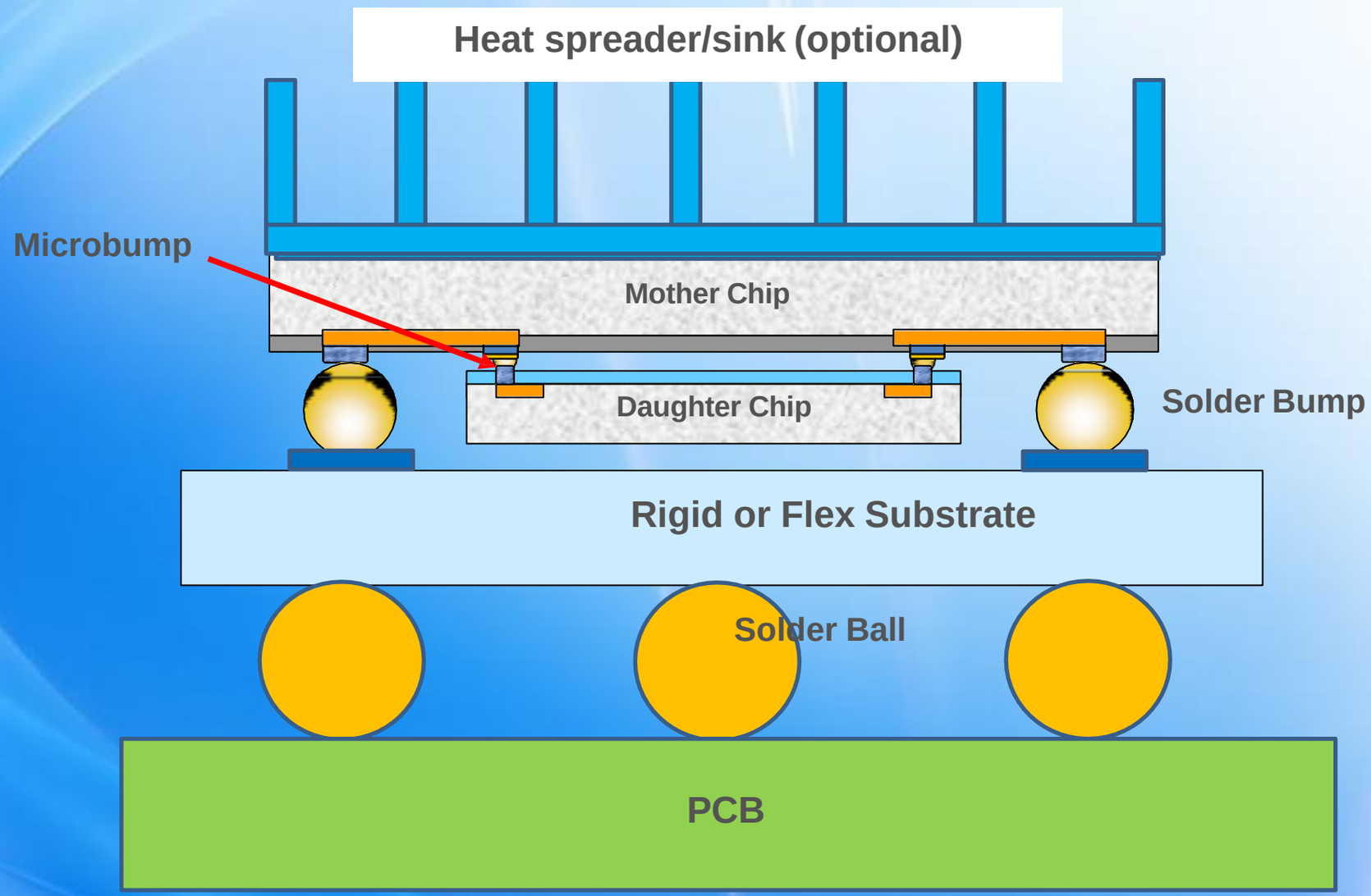
Current Status

- **HVM from ‘2016**



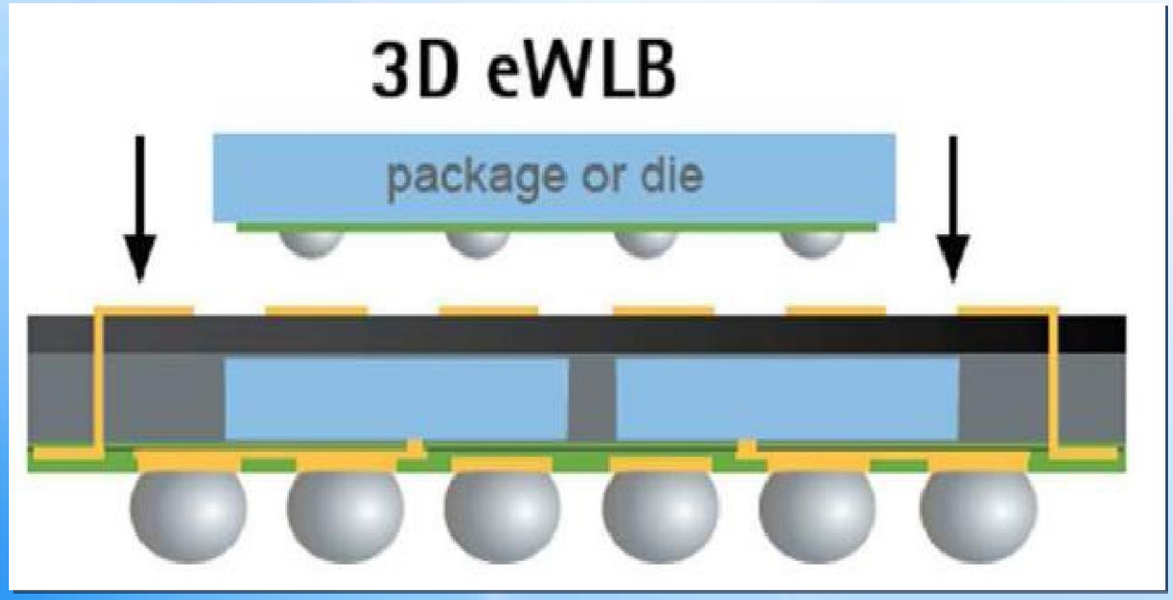


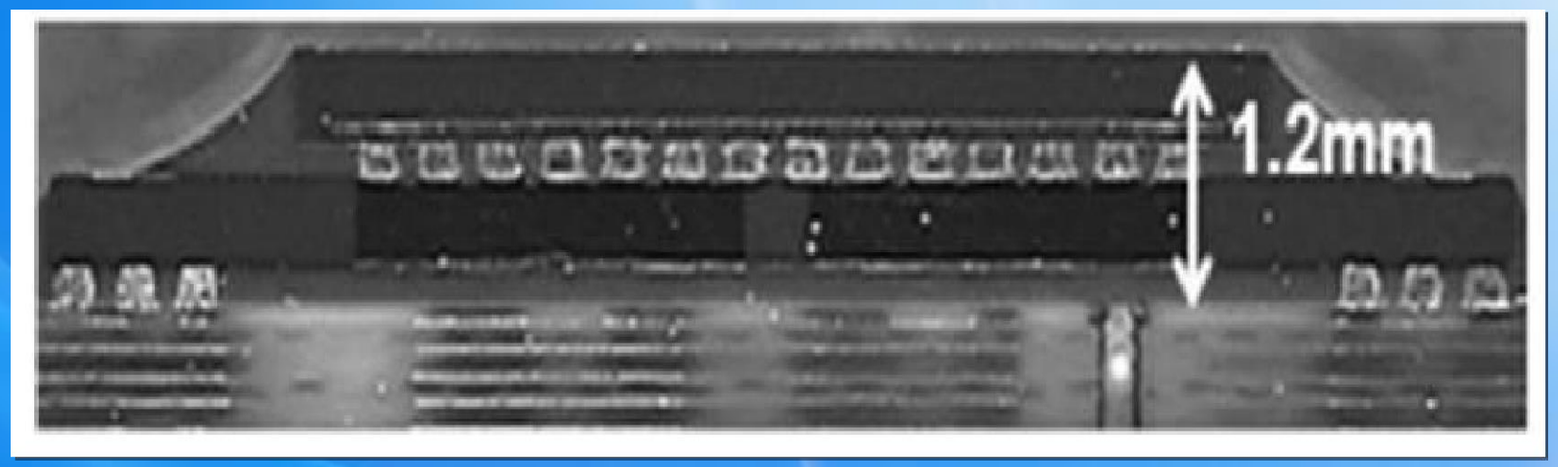
堆疊矽模塊連接在基板上



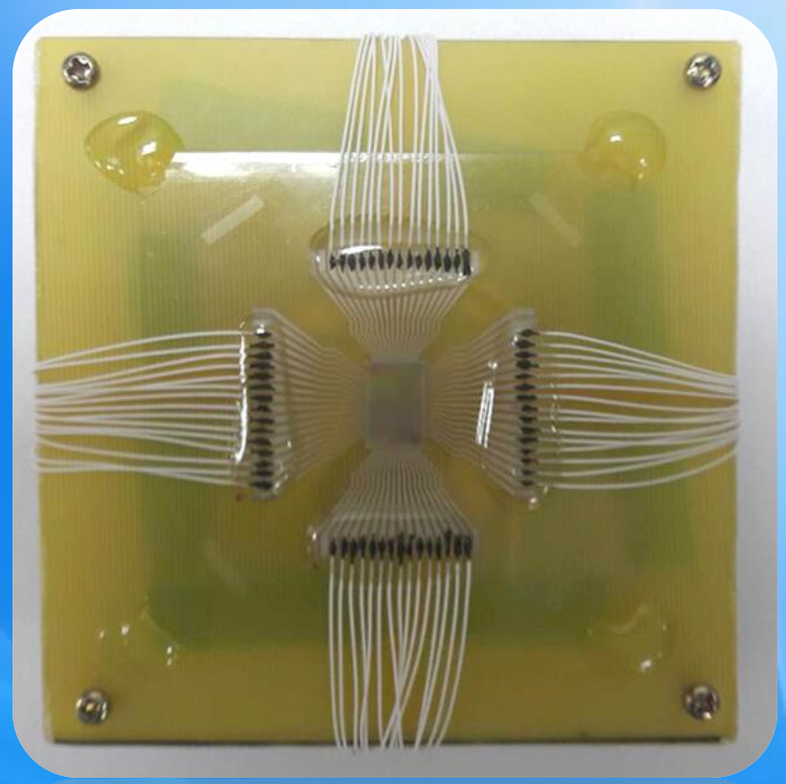
Chip-to-Chip and Face-to-Face

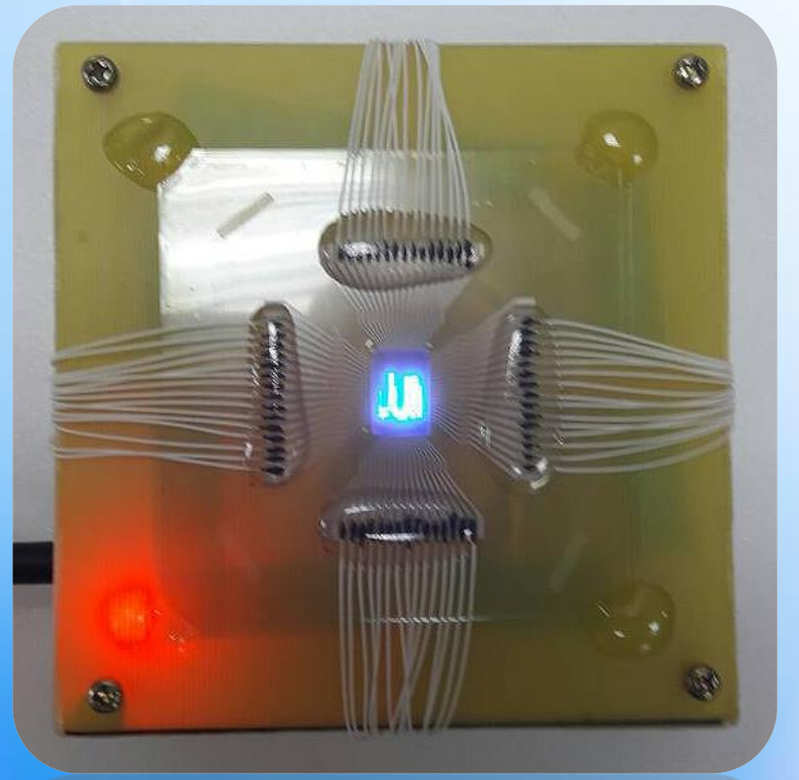
半導體3D堆疊方式





Micro LED 樣品圖





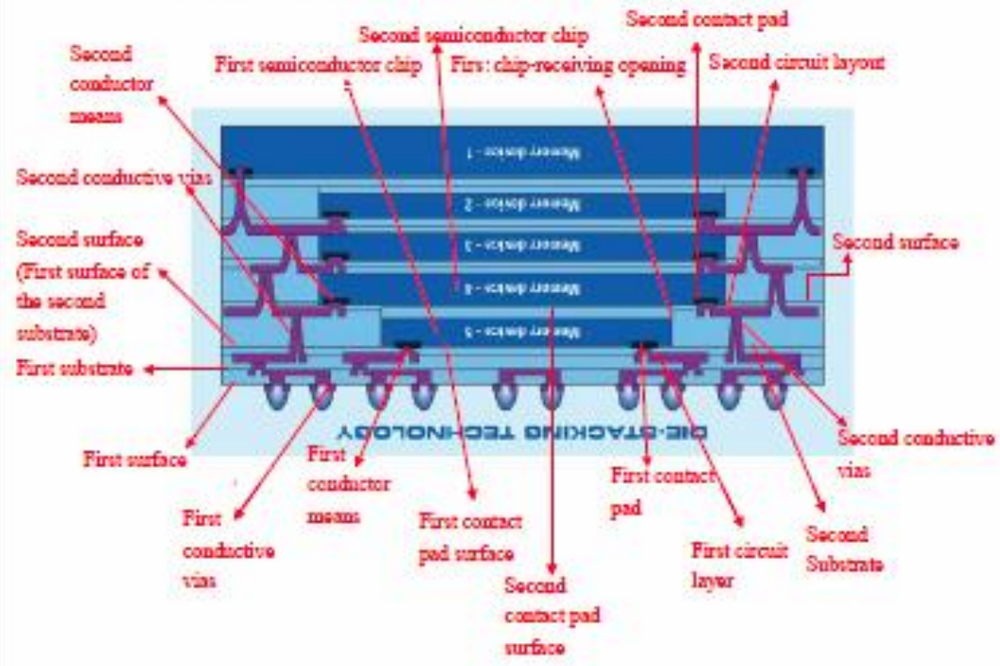
3D封裝專利清單

項目	專利號	案弓名稱
1	US7383630	Method for making a circuit plate
2	US6774473	Semiconductor chip module
3	US6420788	Method for mounting a semiconductor chip on a substrate and semiconductor device adapted for mounting on a substrate
4	US6437448	Semiconductor device adapted for mounting on a substrate
5	US7176573	Semiconductor device with a multi-level interconnect structure and method for making the same
6	I241009	一種形成玄砲凸塊的方法及具布如此形成之電凸塊的裝置
7	I292178	堆疊式半導體晶片封裝體
8	US7411285	Low profile stacked semiconductor chip package
9	ZL200510117763.5	堆疊式半導體晶片封裝體
10	US8076775	Semiconductor package and method for making the same
11	US7672130	Heat dissipating device
12	ZL201110036515.3	散熱裝置

長龍國際專利與台積電堆疊封裝產品的侵權比對

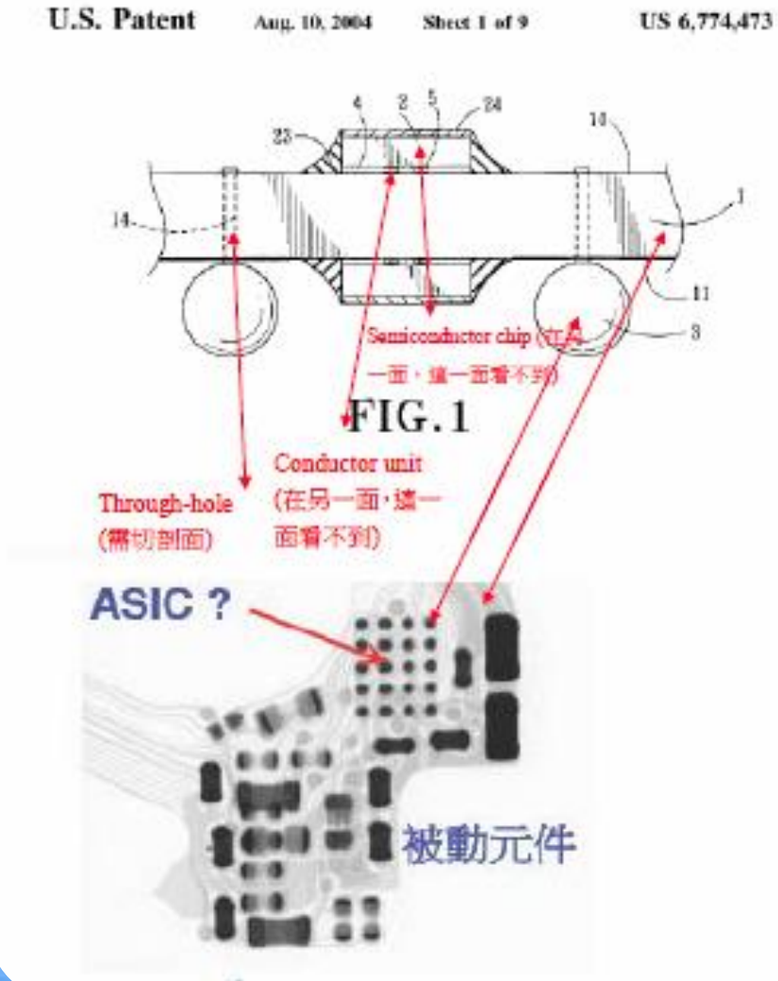
PATENT CLAIM 1 (US6704609)	台積電產品
A multi-chip semiconductor module, comprising:	台積電產品，包含:
A chip-mounting member including first and second substrates;	一個包括 first 和 second substrates 的 chip-mounting member;
Said first substrate having opposite first and second surfaces, a plurality of first conductive vias that extend through said first and second surfaces, and a first circuit layout patterned on said second surface and connected electrically to said first conductive vias;	該 first substrate 具有 first 和 second surfaces，數個貫穿該 first 和 second surfaces 的 first conductive vias，及一在該 second surface 上且是電氣連接至該等 first conductive vias 的 first circuit layout;
Said second substrate having opposite first and second surfaces, a plurality of second conductive vias that extend through said first and second surfaces of said second substrate, a second circuit layout patterned on said second surface of said second substrate and connected electrically to said second conductive vias, and a first chip-receiving opening formed therein;	該 second substrate 具有 first 和 second surfaces，數個貫穿該 second substrate 之 first 和 second surfaces 的 second conductive vias，一在該 second sustrate 之 second surface 上且是電氣連接至該等 second conductive vias 的 second circuit layout，及一 first chip-receiving opening;
Said first surface of said second substrate being bonded on said second surface of said first substrate such that said second circuit layout is connected electrically to said first circuit layout through said first and second conductive vias;	該 second substrate 的 first surface 是黏合在該 first substrate 的 second surface 上以致於該 second circuit layout 是經由 first 和 second conductive vias 來電氣連接到該 first circuit layout
A first semiconductor chip disposed in said first chip-receiving opening and having a first contact pad surface mounted on said second surface of said first substrate, said first contact pad surface being formed with a plurality of first contact pads;	一置於該 first chip-receiving opening 內且具有一 first contact pad surface 安裝在該 first substrate 之 second surface 上的 first semiconductor chip，該 first contact pad surface 是形成有數個 first contact pads;
First conductor means for connecting electrically said first contact pads to said first circuit layout;	用於把該等 first contact pads 電氣連接到該 first circuit layout 的 first conductor means;
A second semiconductor chip having a	一具有一 second contact pad surface 在

second contact pad surface mounted on said second surface of said second substrate, said second contact pad surface being formed with a plurality of second contact pads; and	該 second substrate 之 second surface 上的 second semiconductor chip，該 second contact pad surface 是形成有數個 second contact pads; 及
Second conductor means for connecting electrically said second contact pads to said second circuit layout.	用於把該等 second contact pads 電氣連接到該 second circuit layout 的 second conductor means.



長龍國際專利與日月光代工 APPLE指紋辨識產品的侵權比對

US6774473 與日月光 SiP Side by Side BGA 產品比較



US6774473 專利的申請專利範圍第 1 項

1. A semiconductor chip module comprising:

a chip-mounting member having opposite first and second surfaces a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces;

a first semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;

a first dielectric tape member for bonding adhesively said first semiconductor chip on said chip-mounting member;

a first conductor unit for connecting electrically said contact pads of said first semiconductor chip and said first circuit traces; and

a plurality of solder balls disposed on one of said first and second surfaces of said chip-mounting member, each of said solder balls being aligned with and being connected to a respective one of said plated through holes in said chip-mounting member,

wherein said first circuit traces and said first semiconductor chip are disposed on a same one of said first and second surfaces of said chip-mounting member;

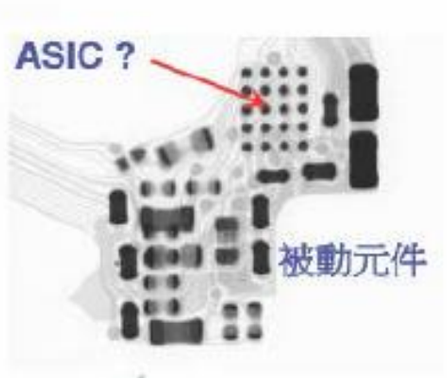
said first dielectric tape member bonds adhesively said pad mounting surface of said first semiconductor chip on said same one of said first and second surfaces of said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said first semiconductor chip; and

said first conductor unit includes a plurality of conductive contact balls that are disposed within said holes in said first dielectric tape member to establish electrical connection between said contact pads of said first semiconductor chip and said first circuit traces.

長龍國際專利與日月光代工 APPLE指紋辨識產品的侵權比對

US6774473 與指紋辨識產品的文字比對

PATENT CLAIM 1 (US6774473)	指紋辨識產品
A semiconductor chip module, comprising:	指紋辨識產品，包含:
A chip-mounting member having opposite first and second surface a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces;	一個 chip-mounting member，該 chip-mounting member 具有 first and second surface, a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces;
A first semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;	一個 first semiconductor chip，其具有一個設有數個 contact pads 的 pad mounting surface;
A first dielectric tape member for bonding adhesively said first semiconductor chip on said chip-mounting member;	一個 first dielectric tape member，其把該 first semiconductor chip 固定在該 chip-mounting member 上;
A first conductor unit for connecting electrically said contact pads of said first semiconductor chip and said first circuit traces; and	一個 first conductor unit，其用於把該 first semiconductor chip 的 contact pads 與該 first circuit traces 電氣連接;
A plurality of solder balls disposed on one of said first and second surfaces of said chip-mounting member, each of said solder balls being aligned with and being connected to a respective one of said plated through holes in said chip-mounting member;	數個 solder balls，其設於該 chip-mounting member 的 second surface, 每個 solder ball 是連接到對應的 plated through hole;
Wherein said first circuit traces and said first semiconductor chip are disposed on a same one of said first and second surfaces of said chip-mounting member;	其中，first circuit traces 與 first semiconductor chip 是置於 chip-mounting member 的 first surface;
Said first dielectric tape member bonds adhesively said pad mounting surface of said first semiconductor chip on said same one of said first and second surfaces of said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said first semiconductor chip; and	該 first dielectric tape member 把該 first semiconductor chip 的 pad mounting surface 固定在該 chip-mounting member 的 first surface 上，而且是形成有數個 hole 在對應於該 first semiconductor chip 的 contact pad 的位置; 及
Said first conductor unit includes a plurality of conductive contact balls that are disposed within said holes in said first dielectric tape member to establish electrical connection between said contact pads of said first semiconductor chip and said first circuit traces.	該 first conductor unit 包括置於該 first dielectric tape member 的 hole 內的 conductive contact balls 以建立在 first semiconductor chip 與 first circuit traces 之間的電氣連接.



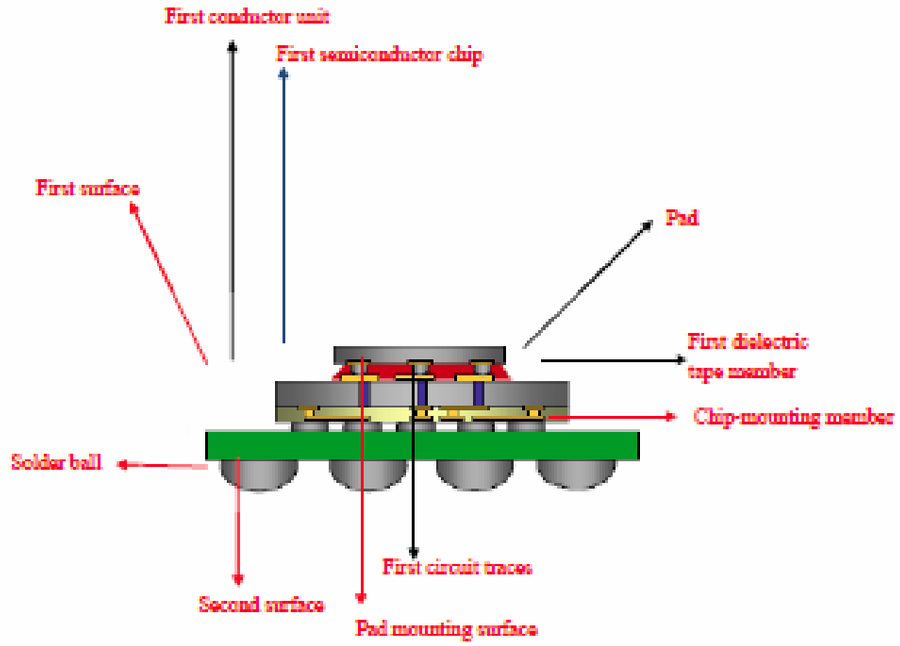
長龍國際專利與SAMSUNG
堆疊封裝的侵權比對

PATENT CLAIM 1 (US8076775)	Samsung 產品
A semiconductor package, comprising:	Samsung 產品, 包含:
A semiconductor substrate having front and rear sides, two opposite lateral sides transverse to said front and rear sides, a pad-mounting face disposed at said front side, and at least one bonding pad formed on said pad-mounting face;	一個 chip-mounting member, 該 chip-mounting member 具有 first and second surface, a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces; (through holes 在圖中沒有被描繪出來，它們的位置就是在 solder ball 的位置，貫穿該 chip-mounting member, 與 first circuit trace 連接)
A first inner insulator layer formed on said pad-mounting face and formed with at least one pad-aligned hole that exposes said bonding pad;	一個 first semiconductor chip, 其具有一個設有數個 contact pads 的 pad mounting surface;
At least one internal wiring connected to said bonding pad, extending therefrom through said pad-aligned hole to said front side of said semiconductor substrate, and further extending from said front side of said semiconductor substrate along one of said lateral sides of said semiconductor substrate to said rear side of said semiconductor substrate, said internal wiring including a first segment formed on said first inner insulator layer, a second segment disposed at said one of said lateral sides of said semiconductor substrate, and a third segment disposed at said rear side of said semiconductor substrate;	一個 first dielectric tape member, 其把該 first semiconductor chip 固定在該 chip-mounting member 上;
A first outer insulator disposed at said front side of said semiconductor substrate and having a portion that is formed on said first segment of said internal wiring and that is formed with at least one first wire-connecting hole which exposes a portion of said first segment of said internal wiring;	一個 first conductor unit, 其用於把該 first semiconductor chip 的 contact pads 與該 first circuit traces 電氣連接;

A second outer insulator layer disposed at said rear side of said semiconductor substrate and having a portion that is formed on said third segment of said internal wiring and that is formed with at least one second wire-connecting hole which exposes a portion of said third segment of said internal wiring;	數個 solder balls, 其設於該 chip-mounting member 的 second surface, 每個 solder ball 是連接到對應的 plated through hole;
A wire-defining layer formed on said first inner insulator layer and formed with at least one wire-defining hole that exposes a portion of said first inner insulator layer, said first segment of said internal wiring extending into and through said wire-defining hole and being formed on said portion of said first inner insulator layer exposed by said wire-defining hole, said first outer insulator layer further having another portion that is formed on said wire-defining layer, wherein said semiconductor substrate further has a rear face disposed at said rear side of said semiconductor substrate, and two opposite side faces disposed at said lateral sides, respectively, and interconnecting said pad-mounting face and said rear face, said second segment of said internal wiring being formed on one of said side faces that is disposed at said one of said lateral sides, said third segment of said internal wiring being formed on said rear face of said semiconductor substrate;and;	其中，first circuit traces 與 first semiconductor chip 是置於 chip-mounting member 的 first surface;
A second inner insulator layer that is formed on said rear face of said semiconductor substrate and that is formed with at least one wire-extension	該 first dielectric tape member 把該 first semiconductor chip 的 pad mounting surface 固定在該 chip-mounting member 的 first surface 上, 而且是形成有數個

長龍國際專利與SAMSUNG堆疊封裝的侵權比對

hole which exposes a portion of said rear face of said semiconductor substrate, said third segment of said internal wiring extending into said wire-extension hole and being formed on said portion of said rear face of said semiconductor substrate exposed by said wire-extension hole, said second outer insulator layer further having another portion that is formed on said second inner insulator layer.	hole 在對應於該 first semiconductor chip 的 contact pad 的位置;及



長龍國際專利與INTEL CPU的侵權比對

PATENT CLAIM 1 (US6774473)	Intel CPU 產品
A semiconductor chip module, comprising:	Intel CPU 產品, 包含:
A chip-mounting member having opposite first and second surface a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces;	一個 chip-mounting member, 該 chip-mounting member 具有 first and second surface, a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces; (through holes 在圖中沒有被描繪出來, 它們的位置就是在 solder ball 的位置, 貫穿該 chip-mounting member, 與 first circuit trace 連接)
A first semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;	一個 first semiconductor chip, 其具有一個設有數個 contact pads 的 pad mounting surface;
A first dielectric tape member for bonding adhesively said first semiconductor chip on said chip-mounting member;	一個 first dielectric tape member, 其把該 first semiconductor chip 固定在該 chip-mounting member 上;
A first conductor unit for connecting electrically said contact pads of said first semiconductor chip and said first circuit traces; and	一個 first conductor unit, 其用於把該 first semiconductor chip 的 contact pads 與該 first circuit traces 電氣連接;
A plurality of solder balls disposed on one of said first and second surfaces of said chip-mounting member, each of said solder balls being aligned with and being connected to a respective one of said plated through holes in said chip-mounting member;	數個 solder balls, 其設於該 chip-mounting member 的 second surface, 每個 solder ball 是連接到對應的 plated through hole;
Wherein said first circuit traces and said first semiconductor chip are disposed on a same one of said first and second surfaces of said chip-mounting member;	其中, first circuit traces 與 first semiconductor chip 是置於 chip-mounting member 的 first surface;
Said first dielectric tape member bonds adhesively said pad mounting surface of said first semiconductor chip on said same one of said first and second surfaces of	該 first dielectric tape member 把該 first semiconductor chip 的 pad mounting surface 固定在該 chip-mounting member 的 first surface 上, 而且是形成有數個

said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said first semiconductor chip; and	hole 在對應於該 first semiconductor chip 的 contact pad 的位置;及
Said first conductor unit includes a plurality of conductive contact balls that are disposed within said holes in said first dielectric tape member to establish electrical connection between said contact pads of said first semiconductor chip and said first circuit traces.	該 first conductor unit 包括置於該 first dielectric tape member 的 hole 內的 conductive contact balls 以建立在 first semiconductor chip 與 first circuit traces 之間的電氣連接.

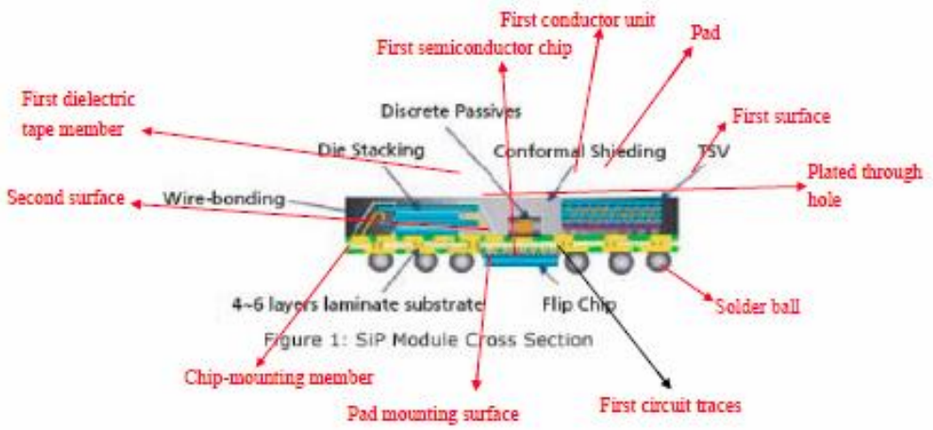
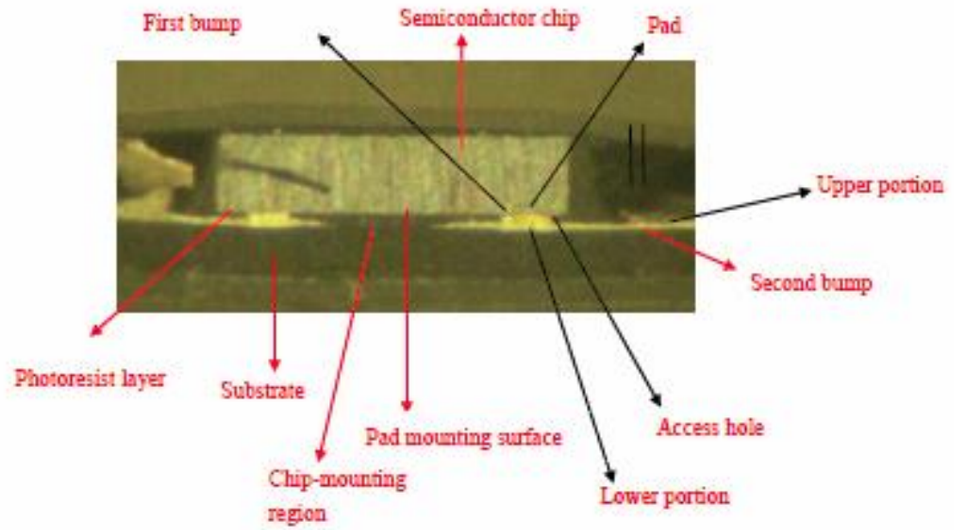


Figure 1: SiP Module Cross Section

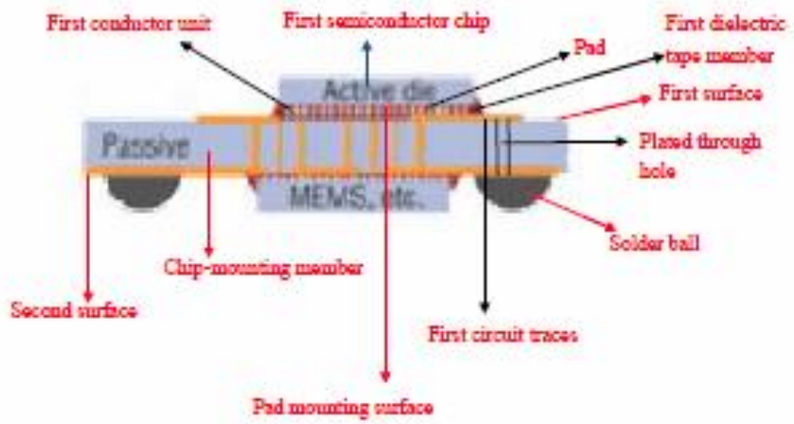
長龍國際專利與ETAG的侵權比對

PATENT CLAIM 1 (US6774473)	ETAG
A semiconductor device adapted for mounting on a substrate, the substrate having a chip-mounting region provided with a plurality of solder points, said semiconductor device, comprising:	ETAG, 包含:
A semiconductor chip having a pad-mounting surface provided with a plurality of bonding pads which are disposed on said pad-mounting surface;	一個 semiconductor chip, 該 semiconductor chip 具有一個設有數個 bonding pad 的 pad-mounting surface;
A plurality of conductive first bumps electrically and respectively connected to and protruding from said bonding pads;	數個電氣地且分別地連接到該等 bonding pads 的 first bump;
A photoresist layer formed on said pad-mounting surface of said semiconductor chip, said photoresist layer being formed with a plurality a access holes registered with and exposing at lest a portion of a respective one of said first bumps on said bonding pads; and	一個形成在該 semiconductor chip 之 pad-mounting surface 上的 photoresist layer, 該 photoresist layer 形成有數個露出對應之 first bump 之一部份的 access holes; 及
A plurality of conductive second bumps, each of which has a lower portion filling a respective one of said access holes to electrically connected with and encapsulate said portion of a respective one of said first bumps, and an upper portion extending from said lower portion and protruding from an upper surface of said photoresist layer opposite to said pad-mounting surface	數個 second bump, 每個 second bump 具有一與對應之 first bump 之該部份電氣連接的 lower portion, 及從該 lower portion 延伸出來且自該 photoresist layer 之 upper surface 突起的 upper portion.

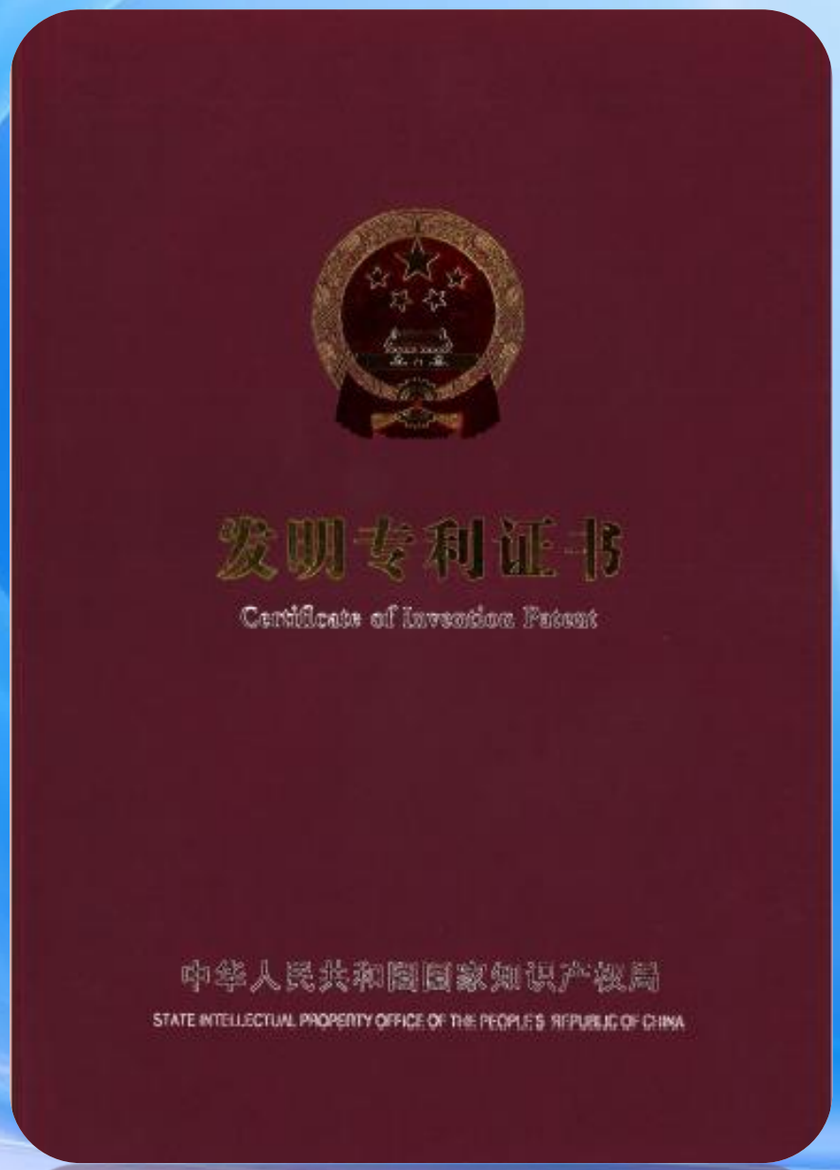


長龍國際專利與台積電堆疊封裝產品的侵權比對

PATENT CLAIM 1 (US6774473)	台積電產品
A semiconductor chip module, comprising:	台積電產品，包含:
A chip-mounting member having opposite first and second surface a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces;	一個 chip-mounting member, 該 chip-mounting member 具有 first and second surface, a set of first circuit traces, and a plurality of plated through holes that extend through said first and second surfaces and that are connected to said first circuit traces; (through holes 在圖中沒有被描繪出來，它們的位置就是在 solder ball 的位置，貫穿該 chip-mounting member, 與 first circuit trace 連接)
A first semiconductor chip having a pad mounting surface with a plurality of contact pads provided thereon;	一個 first semiconductor chip, 其具有一個設有數個 contact pads 的 pad mounting surface;
A first dielectric tape member for bonding adhesively said first semiconductor chip on said chip-mounting member;	一個 first dielectric tape member, 其把該 first semiconductor chip 固定在該 chip-mounting member 上;
A first conductor unit for connecting electrically said contact pads of said first semiconductor chip and said first circuit traces; and	一個 first conductor unit, 其用於把該 first semiconductor chip 的 contact pads 與該 first circuit traces 電氣連接;
A plurality of solder balls disposed on one of said first and second surfaces of said chip-mounting member, each of said solder balls being aligned with and being connected to a respective one of said plated through holes in said chip-mounting member;	數個 solder balls, 其設於該 chip-mounting member 的 second surface, 每個 solder ball 是連接到對應的 plated through hole;
Wherein said first circuit traces and said first semiconductor chip are disposed on a same one of said first and second surfaces of said chip-mounting member;	其中，first circuit traces 與 first semiconductor chip 是置於 chip-mounting member 的 first surface;
Said first dielectric tape member bonds adhesively said pad mounting surface of said first semiconductor chip on said same one of said first and second surfaces of	該 first dielectric tape member 把該 first semiconductor chip 的 pad mounting surface 固定在該 chip-mounting member 的 first surface 上, 而且是形成有數個
said chip-mounting member, and is formed with a plurality of holes at positions registered with said contact pads of said first semiconductor chip; and	hole 在對應於該 first semiconductor chip 的 contact pad 的位置;及
Said first conductor unit includes a plurality of conductive contact balls that are disposed within said holes in said first dielectric tape member to establish electrical connection between said contact pads of said first semiconductor chip and said first circuit traces.	該 first conductor unit 包括置於該 first dielectric tape member 的 hole 內的 conductive contact balls 以建立在 first semiconductor chip 與 first circuit traces 之間的電氣連接.



長龍國際控股的3D封裝相關專利




证书号第550086号

发明专利证书

发明名称：堆叠式半导体芯片封装体

发明人：沈育浓

专利号：ZL 2005 1 0117763.5

专利申请日：2005年11月10日

专利权人：沈育浓

授权公告日：2009年9月16日

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局长 田力普

2009年9月16日

第1页(共1页)

長龍國際控股的3D封裝相關專利

The United States of America

The Director of the United States Patent and Trademark Office

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

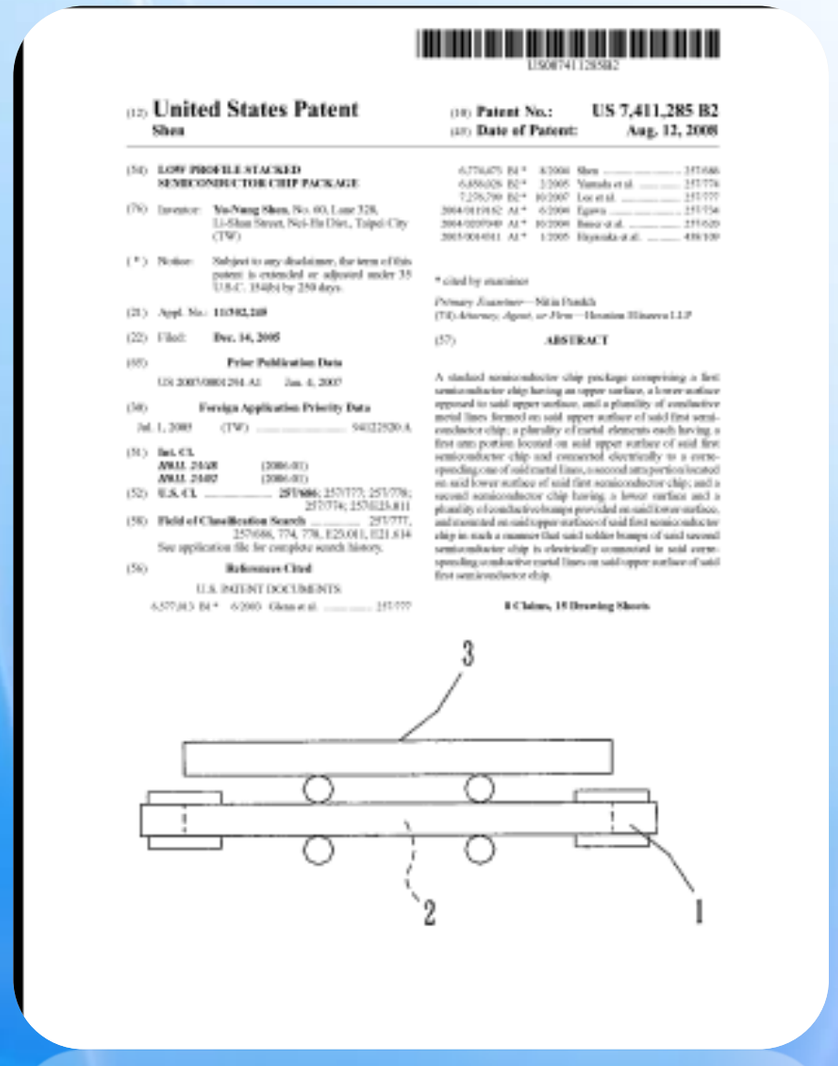
Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America, and if the invention is a process, of the right to exclude others from using, offering for sale or selling throughout the United States of America, or importing into the United States of America, products made by that process, for the term set forth in 35 U.S.C. 154(a)(2) or (c)(1), subject to the payment of maintenance fees as provided by 35 U.S.C. 41(b). See the Maintenance Fee Notice on the inside of the cover.

David J. Kappos

Director of the United States Patent and Trademark Office



US007411285B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 7,411,285 B2**
(45) **Date of Patent: Aug. 12, 2008**

(54) **LOW PROFILE STACKED SEMICONDUCTOR CHIP PACKAGE**

(76) Inventor: **Yu-Nung Shen**, No. 60, Lane 328, Li-Shan Street, Nei-Hu Dist., Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 250 days.

(21) Appl. No.: **11/302,210**

(22) Filed: **Dec. 14, 2005**

(65) **Prior Publication Data**

US 2007/0001294 A1 Jan. 4, 2007

(30) **Foreign Application Priority Data**

Jul. 1, 2005 (TW) ..... 94122920 A

(51) **Int. Cl.**
H01L 23/48 (2006.01)
H01L 23/02 (2006.01)

(52) **U.S. Cl.** **257/686**; 257/777; 257/778; 257/774; 257/E25.011; 257/E23.011

(58) **Field of Classification Search** 257/777, 257/686, 774, 778, E25.011, E23.011
See application file for complete search history.

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Primary Examiner—Nitin Parekh
(74) *Attorney, Agent, or Firm*—Houston Eliseeva LLP

(57) **ABSTRACT**

A stacked semiconductor chip package comprising a first semiconductor chip having an upper surface, a lower surface opposed to said upper surface, and a plurality of conductive metal lines formed on said upper surface of said first semiconductor chip, a plurality of metal elements each having a first area portion located on said upper surface of said first semiconductor chip and connected electrically to a corresponding one of said metal lines, a second area portion located on said lower surface of said first semiconductor chip, and a second semiconductor chip having a lower surface and a plurality of conductive bumps provided on said lower surface, and connected on said upper surface of said first semiconductor chip in such a manner that said solder bumps of said second semiconductor chip is electrically connected to said corresponding conductive metal lines on said upper surface of said first semiconductor chip.

8 Claims, 10 Drawing Sheets

US008076775B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 8,076,775 B2**
(45) **Date of Patent: Dec. 13, 2011**

(54) **SEMICONDUCTOR PACKAGE AND METHOD FOR MAKING THE SAME**

(76) Inventor: **Yu-Nung Shen**, Taipei (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 73 days.

(21) Appl. No.: **12/357,334**

(22) Filed: **Jan. 21, 2009**

(65) **Prior Publication Data**

US 2009/0194863 A1 Aug. 6, 2009

(30) **Foreign Application Priority Data**

Feb. 1, 2008 (TW) ..... 97104403 A

(51) **Int. Cl.**
H01L 23/04 (2006.01)

(52) **U.S. Cl.** . **257/730**; 257/686; 257/774; 257/E23.023; 257/E23.069; 257/E23.125; 438/106; 438/127; 361/777

(58) **Field of Classification Search** 257/686, 257/678, 690, 692, 693, 701, 730, 774, E23.061, 257/E25.023, E23.069, E23.125; 438/106, 438/109, 110, 125, 126, 127; 361/777
See application file for complete search history.

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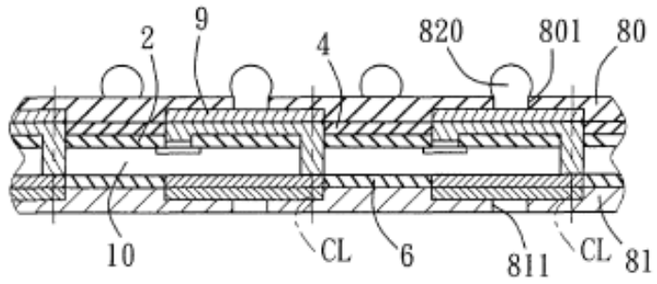
Primary Examiner — William D Coleman
Assistant Examiner — Su Kim
(74) *Attorney, Agent, or Firm* — Christie, Parker & Hale, LLP

(57) **ABSTRACT**

A semiconductor package includes: a semiconductor substrate; an inner insulator layer formed on the substrate; at least one internal wiring extending from a front side of the substrate along one of lateral sides of the substrate to a rear side of the substrate; a first outer insulator layer disposed at the front side of the substrate, formed on the internal wiring, and formed with at least one wire-connecting hole; and a second outer insulator layer disposed at the rear side of the substrate, formed on the internal wiring, and formed with at least one wire-connecting hole which exposes a portion of the internal wiring.

7 Claims, 8 Drawing Sheets



US006774473B1

(12) **United States Patent**
Shen

(10) **Patent No.: US 6,774,473 B1**
(45) **Date of Patent: Aug. 10, 2004**

(54) **SEMICONDUCTOR CHIP MODULE**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/407,284**

(22) Filed: **Sep. 28, 1999**

(30) **Foreign Application Priority Data**

Jul. 30, 1999 (TW) ..... 88212813 U

(51) **Int. Cl.**[7] **H01L 23/02**; H01L 23/34

(52) **U.S. Cl.** **257/686**; 257/778; 257/780; 257/723; 257/774; 257/782; 257/783

(58) **Field of Search** 257/686, 725, 257/738, 780, 782, 783, 778, 777, 774

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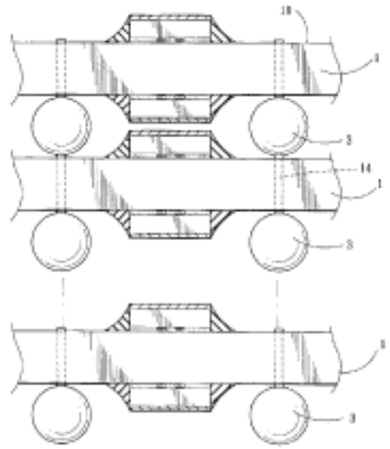
Primary Examiner—Steve Loke
Assistant Examiner—Nitin Parekh
(74) *Attorney, Agent, or Firm*—Merchant & Gould, P.C.

(57) **ABSTRACT**

A semiconductor chip module includes a chip-mounting member having opposite first and second surfaces, a set of circuit traces, and a plurality of plated through holes that extend through the first and second surfaces and that are connected to the circuit traces. A dielectric tape member bonds adhesively a semiconductor chip on the chip-mounting member. A first conductor unit connects electrically contact pads on a pad mounting surface of the semiconductor chip and the circuit traces. A plurality of solder balls are disposed on one of the first and second surfaces of the chip-mounting member, are aligned with and are connected to the plated through holes in the chip-mounting member, respectively.

8 Claims, 9 Drawing Sheets



US007176573B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 7,176,573 B2**
(45) **Date of Patent: Feb. 13, 2007**

(54) **SEMICONDUCTOR DEVICE WITH A MULTI-LEVEL INTERCONNECT STRUCTURE AND METHOD FOR MAKING THE SAME**

(76) Inventor: **Yu-Nung Shen**, 4F, No. 52, Sec. 2, Chang-Shan N. Rd., Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/716,948**

(22) Filed: **Nov. 19, 2003**

(65) **Prior Publication Data**

US 2004/0135257 A1 Jul. 15, 2004

(30) **Foreign Application Priority Data**

Nov. 22, 2002 (TW) ..... 91134054 A

(51) **Int. Cl.**
H01L 23/48 (2006.01)

(52) **U.S. Cl.** **257/758**

(58) **Field of Classification Search** 257/758, 257/734–738, 700; 438/118
See application file for complete search history.

(56) **References Cited**

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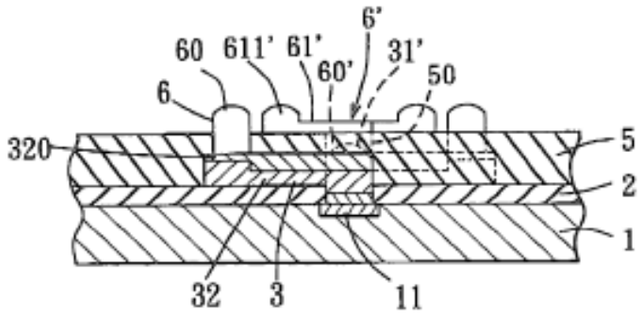
Primary Examiner—Nathan W. Ha

(57) **ABSTRACT**

A semiconductor device includes a semiconductor die and a multi-level interconnect structure that has a first insulating layer formed on the die, conductive horizontal bodies, each of which is connected to a respective bonding pad of the die and has an extension formed on the first insulating layer, a second insulating layer formed on the first insulating layer, and conductive vertical bodies, each of which is connected to the extension of a respective conductive horizontal body and extends through the second insulating layer.

20 Claims, 4 Drawing Sheets



US007383630B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 7,383,630 B2**
(45) **Date of Patent: Jun. 10, 2008**

(54) **METHOD FOR MAKING A CIRCUIT PLATE**

(76) Inventor: **Yu-Nung Shen**, 4F, No. 52, Sec. 2, Chang-Shan N. Rd., Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 312 days.

(21) Appl. No.: **11/166,058**

(22) Filed: **Jun. 24, 2005**

(65) **Prior Publication Data**

US 2006/0000635 A1 Jan. 5, 2006

(30) **Foreign Application Priority Data**

Jun. 30, 2004 (TW) ..... 93119684 A

(51) **Int. Cl.**
H01K 3/10 (2006.01)
H05K 3/02 (2006.01)

(52) **U.S. Cl.** **29/852**; 29/835; 29/846; 29/847; 29/848

(58) **Field of Classification Search** 29/835, 29/846, 847, 848, 852
See application file for complete search history.

(56) **References Cited**

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2001/0040298 A1 * 11/2001 Sakassi et al. 257/737

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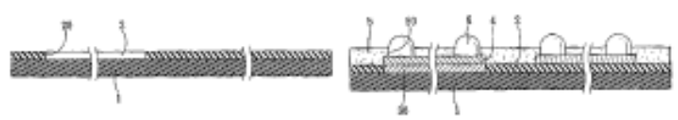
Primary Examiner—C. J Arbes
(74) *Attorney, Agent, or Firm*—Ladas and Parry LLP

(57) **ABSTRACT**

A method for making a circuit plate includes: forming first holes in an insulating layer; forming a conductive layer on the insulating layer such that a portion of the conductive layer fills the first holes; grinding the conductive layer such that the portion of the conductive layer remains in the first holes to form a pattern of conductive traces; forming a dielectric protective layer that covers the insulating layer and the conductive traces; forming a pattern of second holes in the protective layer such that a portion of each of the conductive traces is accessible through a respective one of the second holes; and forming conductive bumps that are respectively connected to the conductive traces.

14 Claims, 5 Drawing Sheets



US007383630B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 7,383,630 B2**
(45) **Date of Patent: Jun. 10, 2008**

(54) **METHOD FOR MAKING A CIRCUIT PLATE**

(76) Inventor: **Yu-Nung Shen**, 4F, No. 52, Sec. 2, Chung-Shan N. Rd., Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 312 days.

(21) Appl. No.: **11/166,058**

(22) Filed: **Jun. 24, 2005**

(65) **Prior Publication Data**

US 2006/0000635 A1 Jan. 5, 2006

(30) **Foreign Application Priority Data**

Jun. 30, 2004 (TW) ..... 93119684 A

(51) **Int. Cl.**
H01K 3/10 (2006.01)
H05K 3/02 (2006.01)

(52) **U.S. Cl.** **29/852**; 29/835; 29/846; 29/847; 29/848

(58) **Field of Classification Search** 29/835, 29/846, 847, 848, 852

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

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7,174,638 B2 * 2/2007 Hsu et al. 29/842
2001/0040298 A1 * 11/2001 Sakurai et al. 257/737

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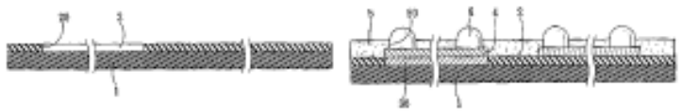
Primary Examiner—C. J Arbes
(74) *Attorney, Agent, or Firm*—Ladas and Parry LLP

(57) **ABSTRACT**

A method for making a circuit plate includes: forming first holes in an insulating layer; forming a conductive layer on the insulating layer such that a portion of the conductive layer fills the first holes; grinding the conductive layer such that the portion of the conductive layer remains in the first holes to form a pattern of conductive traces; forming a dielectric protective layer that covers the insulating layer and the conductive traces; forming a pattern of second holes in the protective layer such that a portion of each of the conductive traces is accessible through a respective one of the second holes; and forming conductive bumps that are respectively connected to the conductive traces.

14 Claims, 5 Drawing Sheets



US006437448B1

(12) **United States Patent**
Chen

(10) **Patent No.: US 6,437,448 B1**
(45) **Date of Patent: Aug. 20, 2002**

(54) **SEMICONDUCTOR DEVICE ADAPTED FOR MOUNTING ON A SUBSTRATE**

(76) Inventor: **I-Ming Chen**, No. 60, Lane 328, Li-Shan St., Nei-Hu Dist., Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/765,793**

(22) Filed: **Jan. 18, 2001**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/725,431, filed on Nov. 29, 2000.

(30) **Foreign Application Priority Data**

Oct. 21, 2000 (TW) ..... 89108578 A

(51) **Int. Cl.**[7] **H01L 23/48**; H01L 23/52; H01L 29/40

(52) **U.S. Cl.** **257/777**; 257/737

(58) **Field of Search** 257/737, 738, 257/777, 778, 779, 780, 781, 782, 784, 787

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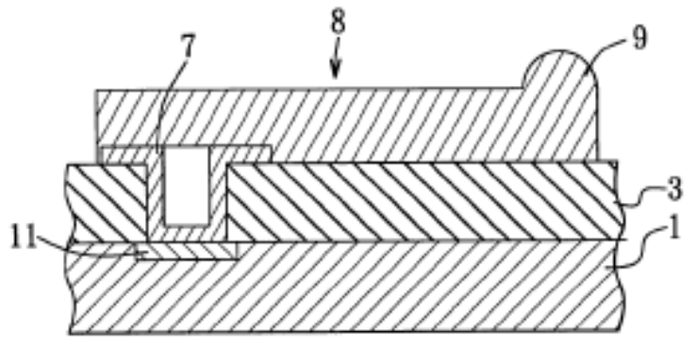
Primary Examiner—Viet Q. Nguyen
Assistant Examiner—David Nhu
(74) *Attorney, Agent, or Firm*—Christensen O'Connor; Johnson Kindness PLLC

(57) **ABSTRACT**

A method for manufacturing a semiconductor device includes the steps of providing a semiconductor chip having a pad-mounting surface with a bonding pad, forming a first bump on the bonding pad, forming a photoresist layer on the pad-mounting surface, forming a second bump which protrudes from the first bump through an upper surface of the photoresist layer, and forming a conductive body on the second bump. The conductive body has an anchor portion connecting electrically with and encapsulating an upper portion of the second bump, and a contact portion offset from the anchor portion and adapted to be connected to a substrate.

11 Claims, 4 Drawing Sheets




US007672130B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 7,672,130 B2**
(45) **Date of Patent: Mar. 2, 2010**

(54) **HEAT DISSIPATING DEVICE**

(76) Inventor: **Yu-Nung Shen**, No. 60, Lane 328 Li-Shan Street, Nei-Hu District, Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **12/229,971**

(22) Filed: **Aug. 27, 2008**

(65) **Prior Publication Data**

US 2009/0059527 A1 Mar. 5, 2009

(30) **Foreign Application Priority Data**

Aug. 31, 2007 (TW) ..... 96214647 U

(51) **Int. Cl.**
H05K 7/20 (2006.01)

(52) **U.S. Cl.** **361/699**; 361/700; 165/104.21; 165/148; 165/165; 422/129

(58) **Field of Classification Search** 361/695, 361/699, 700, 704

See application file for complete search history.

(56) **References Cited**

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2006/0165570 A1 * 7/2006 Knopf et al. 422/224

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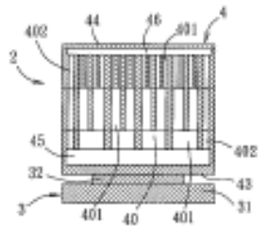
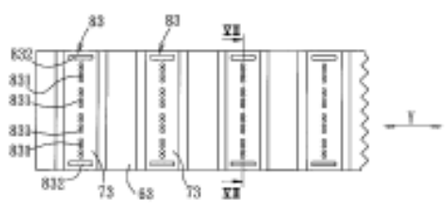
Primary Examiner—Jayprakash N Gandhi
Assistant Examiner—Courtney Smith
(74) *Attorney, Agent, or Firm*—Townsend and Townsend and Crew, LLP

(57) **ABSTRACT**

A heat dissipating device includes a sealed container having hollow floors and floor-spacing assemblies. Each floor-spacing assembly includes hollow spacing walls. Each hollow spacing wall extends from a respective hollow floor and is spaced apart from an adjacent one of the hollow spacing walls of an adjacent one of the floor-spacing assemblies by an air gap. Each two adjacent ones of the hollow floors are interconnected through the hollow spacing walls disposed therebetween. The sealed container defines a liquid reservoir, a condensate reservoir, and a plurality of fluid passages extending through the hollow spacing walls and the hollow floors that are disposed between the liquid reservoir and the condensate reservoir.

9 Claims, 6 Drawing Sheets





THANK YOU!