长龙国际股份有限公司

与新马地区、上海地区合作
启动先进的HBM半导体
COWOS的3D封装项目

https://clisemi.com/

公司简介

长龙国际设立于 2017 年 1 月，我们的团队专注于先进封装厂的整厂输出及绿能技术开发，从技术开发到生产实施。拥有的技术发明基础上，汇聚了一群半导体及绿能领域的专家，确保项目技术先进性和生产高效。

公司沿革

2017 年　　公司成立

2017 年至2020 年　HBM/3D封装及专利布局。

和韓國Pro Test销售额 5000 万美元/每年约150人。

及 ITEST(艾特半导体) 销售额1.2亿美元/每年约 850人。

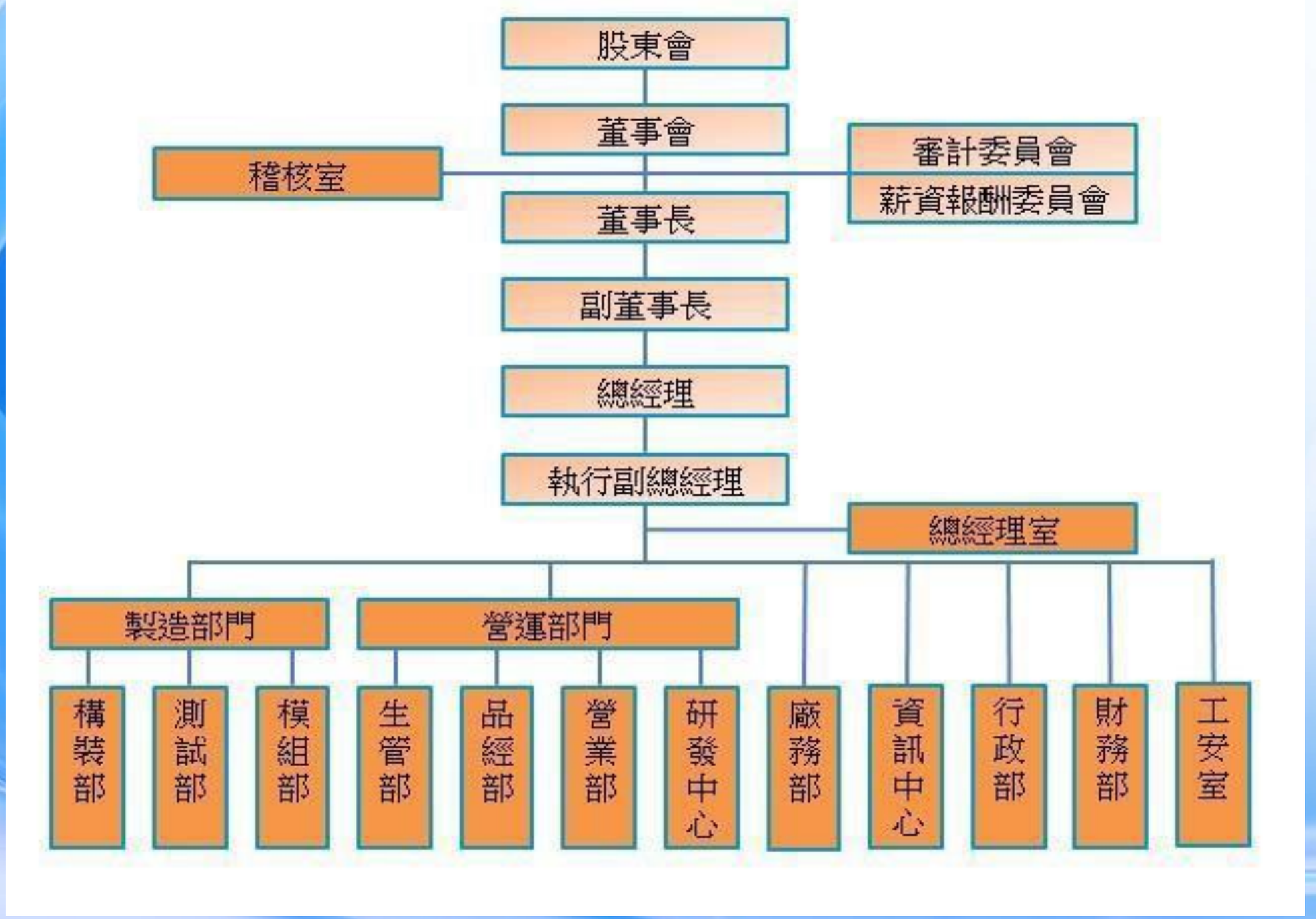
2021 年　　研发增程摩托车。

2022 年　　研发电动脚踏车。

2023 年至2024年　研发无人机增程动力系统。

2025年　　研发机器人动力增程背包专利。

公司组织结构


股東會
董事會
稽核室
審計委員會
薪資報酬委員會
董事長
副董事長
總經理
執行副總經理
總經理室
製造部門
營運部門
構裝部
測試部
模組部
生管部
品經部
營業部
研發中心
廠務部
資訊中心
行政部
財務部
工安室

团队成员

团队	成员	学经历	其它
运营团队	5~7 人		经由董事会聘任
生产技术专家团队	50~70 人		台湾/韩国现职工程师
品质管理专家团队	15~25 人		台湾/韩国现职工程师
市场分析专家	7~9 人		台湾现职工程师

台湾技术团队成员及其经历介绍

职称	姓名	个人经历
技术总监	沈明东	超过 30 年半导体组件封装、电子电路设计、电池材料研发经验
资深顾问	杨博士	清华大学材料科技博士学位 剑桥大学锂电池博士学位
营运执行长	林福男	大同工学院 学士 大同股份有限公司 开发、设计、生产、管理经验 35 年以上
资深工程师	王先生	首席技术总监 开发设计经验 15 年以上 半导体封测研发经验 10 年以上

韩国 技术团队：由多名研发工程师组成， 具有丰富的HBM技术研发和应用经验

HBM Project(Packaging& Test)

1) Basic personal composition(Packaging)

NAME	CAREER	WORK EXPERENCE	REMARK
JJKIM	about 30 Years	SK Hynix& AT semicon	Gensral Affairs
LEE	about 15 Years	SK Hynix Substrate Process	eng'rs
Park	about 5 Years	SK Hynix Substrate Process	eng'rs
KIM	about 10 Years	SK Hynix Bumping	Preocess eng'rs
CHA	about 6 Years	SK Hynix/Domestic Fabless Bumping Process	eng'rs
LEE	about 10 Years	SK Hynix Interpose Process	eng'rs
KIM	about 10 Years	SK Hynix & OSAT HBM Process	eng'rs
KIM	about 10 Years	SK Hynix & OSAT HBM Process	eng'rs
Others(4people)	about 5 Years	Domestic OSAT Assistant	

HBM Project(Packaging& Test)

2) Basic personal composition(Test)

NAME	CAREER	WORK EXPERENCE	REMARK
JJKIM	about 30 Years	SK Hynix& AT semicon	Gensral Affairs (Duplicated)
LEE	about 15 Years	SK Hynix Dram Test	eng'rs
LEE	about 10 Years	SK Hynix	Nand Test eng'rs
JOUNG	about 10 Years	OSAT or Domestic Fabless Logic Test	eng'rs
KIM	about 5 Years	Domestic Fabless or Design Comany	Logic Test eng'rs
Others(3 people)	about 5 Years	Domestic OSAT Assistant	

3) Detail plan

- Establish detailed strategies for each step(Prepare a Test base in conjunction with 3D Packaging development)
- The Test Engineer composition is centered on local personnel, and additional personnel are prepared for early SET UP, Yiled up,etc.
- Separate establishment of overall personal paln,etc.(Engineering/Maintenance/Production.etc)

核心团队：包括多名在半导体行业有多年经验的技术专家和市场营销专家，其中CTO在内存技术研发领域有超过20年的经验。

Pro Test和ITEST(AT semicon)前董事長履歷

Personal Career

個人情報

姓名：金 鎭宙(KIM JIN JOO),63歲

學 歷

- 漢陽大學校 電氣工學科(工學士)
- 漢陽大學校 大學院 電氣工學科(工學碩士)

主要 經力

1986~2002：LG半導體 Test技術 室長
2003~2019：AT semicon 代表理事
2019~2021：HYTC Advisor
2021~現在：KH TECH 代表理事

Detail Career

1986~2002 LG半導體

- Memory Test Program開發& Development Engineer
- Memory(Dram/Nand)/MCU/C MOS image semsor/ASIC Test Eng'rs Team Leader
- 72M Rambus DRAM 國內 最初 Test Program開發

2003~現在 Pro Test/I TEST/AT semicon/KH TECH

2002. Pro Test設立/Test House事業開始
2006. I TEST合併
- Dram&Flash Memory(SK Hynix),System LSI(Samsung),Fabless會社 Test實施

2007. Multi Chip Test & AP Chip Test 開始
2011. 韓國 KOSDAQ上場
2012. Mobile用 DRAM Test實施
2014. Semitech引受合併
- Package and Test House 事業擴大

2019~現在 半導體 Consultanting

HBM項目領導人

韩国技术团队成员及其经历介绍

职称	姓名	个人经历
经理兼董事	GM KIM(Director)	研发部 (另带领约 10 干部成员)
经理	HJ KIM	生技部 (另带领约 50 成员)
经理	CJ Sung	量测部 (另带领约 15 成员)
经理	BHKIM	质量管理部 (另带领约 15 成员)
经理	GH Shin	设备部 (另带领约 12 成员)

商业计划

1. 全面的 日程

1 ）日程安排 经过 部门

item	Detail schedule	Remark
Establish a specific plan	→ 1~2 Week	
Equipment ordering/receiving	→ About3~4Month	
Secure Key Man	→ About 2Month	
Human Resources and Training	→ About 3Month	
Overall production management	→ About 2Month	
1Line set up	→ About 2 Weeks	
Customer Qual	→ About 2~3 Weeks	
General preparation(computer.etc)	→ About 2~3 Weeks	
Others		

2 ）考虑 这 总体日程安排如下 作为 这 工厂 完成 时间表和 设备 介绍，这是 可能的 到 缩短 这 日程。

- 它 有可能 到 缩短 这 日程 时期 当 详细的 计划 已建立 和 这 设备订购单 已推广。

2. 投资 数量 和 必需的 区域

1 ）投资 数量（ 1 线路设置 & 附加计划 ）和 需要区域

Division		1 Line set up	Additional equipment	Total amount
Ivnestment amount	Packaging	USD 7.7M$	USD 34.6M$	USD 42.3M$
	TEST	USD 6.4M$	USD 7.7M$	USD 14.0$
	sum	USD 14.0M$	USD 42.3M$	***USD 56.3M$***
Area required	PKG	Clean room 3,300m²	Clean room 8,250m²	Clean room 11,550m²
	TEST	Clean room 1,650m²	Clean room 1,650m²	Clean room 3,300m²
	etc(Office)	660m²		660m²
	etc(education)	990m²		990m²
	Total required			Total 16,500m²

Note *) Class division is 50% prepared for class 1000 and 10,000

2 ） 这 全部的 投资 是美元 5630万美元 和 这 所需面积为16 , 50 0 ㎡

3. 销售量 和 操作 利润

1） 销售量 和 操作 利润（基于 在 年）

Division		1 Line set up	Additional equipment	Total amount
Sales	Packaging	USD 16.9M$	USD 83.1M$	USD 100.0M$
	TEST	USD 2.3M$	USD 2.6M$	USD 5.0$
	sum	USD 19.2M$	USD 89.2M$	***USD 105.0M$***
Operating profit		8.30%	24.30%	21.30%

Note *1) Sales will be made after normal set up is completed.

*2) Equipment deprecication is calculated on a 5-year straight-line basis.

*3) The material cost of packaging is assumed to be 60%.

2） 和 额外的 投资， 这 速度 返回 预计 到 是 大约 20% 到期的 到 规模经济。

技术优势分析

长龙的3D PoP和3D WLP技术具有显着的替代潜力：

- 3D PoP凭借其多层堆叠和高密度互连结构，适合作为SoIC的替代方案，

尤其在高性能计算和 5G基站等高带宽需求的应用中。

- 3D WLP则以较高的良率和较简化的散热设计，能够替代WoW，

特别适合对芯片面积利用率和 密度要求较高的场景。

表：台积电先进封装工艺与公司技术对比

封装技术	技术全称	特点与优势	适用场景	可对比技术
CoWoS	Chip-on-Wafer-on-Substrate	提供高带宽互连和高效热管理，适合高性能计算；常用于2.5D封装	高性能计算、AI应用（如GPU、高性能处理器）	
InFO	Integrated Fan-Out	无基板扇出型封装，适合移动和IoT设备，封装薄、信号传输性能优越，提升晶圆利用率	移动处理器、IoT设备	
SoIC	System on Integrated Chips	3D堆叠封装技术，支持多芯片垂直堆叠，带来更高系统集成度和更低功耗，减少延迟	高性能计算、5G基站	**长龙 3D PoP (有FAB条件限制)**
WoW	Wafer-on-Wafer	晶圆直接堆叠技术，提高芯片面积 利用率，增强密度 集成，适合高密度 需求	高密度集成应用	**长龙 3D WLP**
TSMC-3DFabric™ Platform	TSMC-SoIC and TSMC-3DFabric™ Platform	集成多个封装技术（如SoIC、CoWoS和InFO），提供2D、2.5D和3D封装的定制化选择，提高整体系统性能	人工智能、5G、云计算、高性能计算应用	

3D WLP 多层堆叠封装

3D WLP 多层堆叠封装在结构上融合了 WLP 和 WoW 的优势，具有较高的带宽密度和较短的互连 路径，同时在性能与功耗之间取得平衡。其散热需求与 WoW 相当，适用于高性能计算、AI 芯片和 5G 基站等场景，并提供了比单层 WLP 更高的集成度。3D WLP 的工艺复杂性和技术难度与 WoW 相当，生产良率也接近 WoW，使其在高性能需求应用中成为 WoW 的替代方案，有助于满足数据 密集型和大规模量产需求。

表：长龙 3D WLP 与 WLP 和 WoW 封装技术特性对比

特性	WoW（Wafer-on-Wafer）	3D WLP（多层堆叠 WLP）	WLP（Wafer Level Packaging）
封装方式	晶圆堆叠封装，将两个或多个完整的晶圆直接垂直堆叠	多层堆叠封装，通过在WLP基础上进行多层垂直堆叠，兼具WLP的封装薄型化特点与WoW的3D堆叠特性	晶圆级封装，在晶圆制造阶段直接封装芯片
封装结构	3D堆叠封装；通过垂直堆叠晶圆实现高密度集成	3D堆叠封装，多层结构使芯片面积利用率提高；可通过垂直互连方式实现多层电路的高效连接	2D封装；单层封装在单一平面上
集成度	高集成度；支持复杂系统级封装和高密度集成	中高集成度；相比传统WLP更高密度，但通常不及完全的3D堆叠封装如WoW的集成度	集成度较低；适合较小封装尺寸需求
性能特点	提供高带宽低延迟互连，适合高性能和大数据吞吐需求	通过垂直堆叠带来较高的带宽密度和更短的互连路径；在性能和功耗之间提供平衡，适合性能和功耗要求适中的应用	较低的互连密度和带宽，适用于低功耗和中等性能需求
散热能力	较高散热需求，适合高性能应用，通常需要更复杂的散热设计	相较于单层WLP具有更高的散热需求，但由于封装较薄通常比WoW的散热设计更为简化，可通过外部散热方案进行优化	散热能力较低，由于封装较薄适合低至中功耗设备

特性	WoW（Wafer-on-Wafer）	3D WLP（多层堆叠WLP）	WLP（Wafer Level Packaging）
应用场景	高性能计算、AI芯片、5G基站等需要高性能的数据应用	高性能计算、AI芯片、5G基站等与WoW相同的高性能需求应用，专为数据密集型和高吞吐量场景设计	移动设备、IoT、低功耗芯片
技术难度	技术要求较高，研发和量产成本较高	技术难度与WoW相当，具有较高的工艺复杂性，但基于WLP平台发展，使其在量产稳定性上有所保障	工艺较为成熟，适合大规模量产
生产良率	量产良率相对较低，适合小批量高性能应用	生产良率与WoW相当，设计用于大规模量产，并可作为WoW的替代方案，以提供相似性能的封装选择	高良率，已成熟应用于消费电子和移动芯片生产

专利布局

长龙的专利布局涵盖了半导体封装、低轮廓结构、散热装置及多层互连结构等核心领域，体现了其 在高密度集成、散热管理和低轮廓封装等关键技术上的优势。例如，涵盖了多层集成和电气连接优 化方法，为高性能需求提供了稳健的基础；而散热相关专利则确保了高集成度芯片的热管理效率。 整体布局支持长龙在先进封装领域的竞争力，并有助于进一步优化其产品性能和市场覆盖。

表：与先进封装有关专利 (标记为主专利)

Item	Patent Number	Patent Name	Publication Date
1	US 677	onductor chip module	1999/9/28
2	US 642	d for mounting a semiconductor chip on a ate and semiconductor device adapted for ng on a substrate	2000/10/16
3	US 670		2000/7/18
4	US 662		2000/8/4
5	US 643	onductor device adapted for mounting on a ate	2001/1/18
6	US 657		2001/11/13
7	US 658		2001/11/13
8	US 673		2001/3/16
9	US 660	d for mounting a semiconductor chip on a ate and semiconductor device adapted for ng on a substrate	2002/4/11
10	US 661	d for mounting a semiconductor chip on a ate and semiconductor device adapted for ng on a substrate	2002/4/17
11	US 667		2003/1/8
12	US 771		2003/11/19
13	US 768		2003/11/19
14	US 124		2003/5/12

Item	Patent Number	Patent Name	Publication Date
15	US 652	[redacted]	2003/6/26
16	US 721		2004/4/28
17	ZL 200		2005/11/13
18	US 754		2005/12/14
19	US 738		2005/6/24
20	US 129		2005/7/1
21	M3289		2007/3/1
22	US 767		2008/8/27
23	US 807		2009/12/1
24	ZL 201		2017/1/31

长龙在2002年形成了针对 substrate 的关键专利布局，锁定了多个涉及芯片在基板上的安装方法与 封装结构的专利，这些早期的创新限制了其他大厂的技术路线。专利相继发布，进一步巩固了长龙 在基板相关技术的市场优势。这些专利的布局确保了在多芯片模块的封装和安装方法上，长龙在行 业中保持先发地位，对其他大厂在相关领域的技术开发造成了显着限制。

主要专利对3D WLP和3D PoP的发展优势

作为3D WLP和3D PoP发展的关键技术布局，长龙的专利组合增强了其在多层封装中的优势：

- 提升了电气连接和安装精度，优化了多层封装的连接可靠性；
- 微细互连技术则在多芯片模块中提升了结构灵活性和稳定性；
- 通过简化工艺和优化电气连接，提高了3D精密封装的效率；
- 多层互连结构则专注于高密度需求，尤其适合3D WLP的应用。这些布局奠定了长龙在3D封装**领域的稳固地位。**

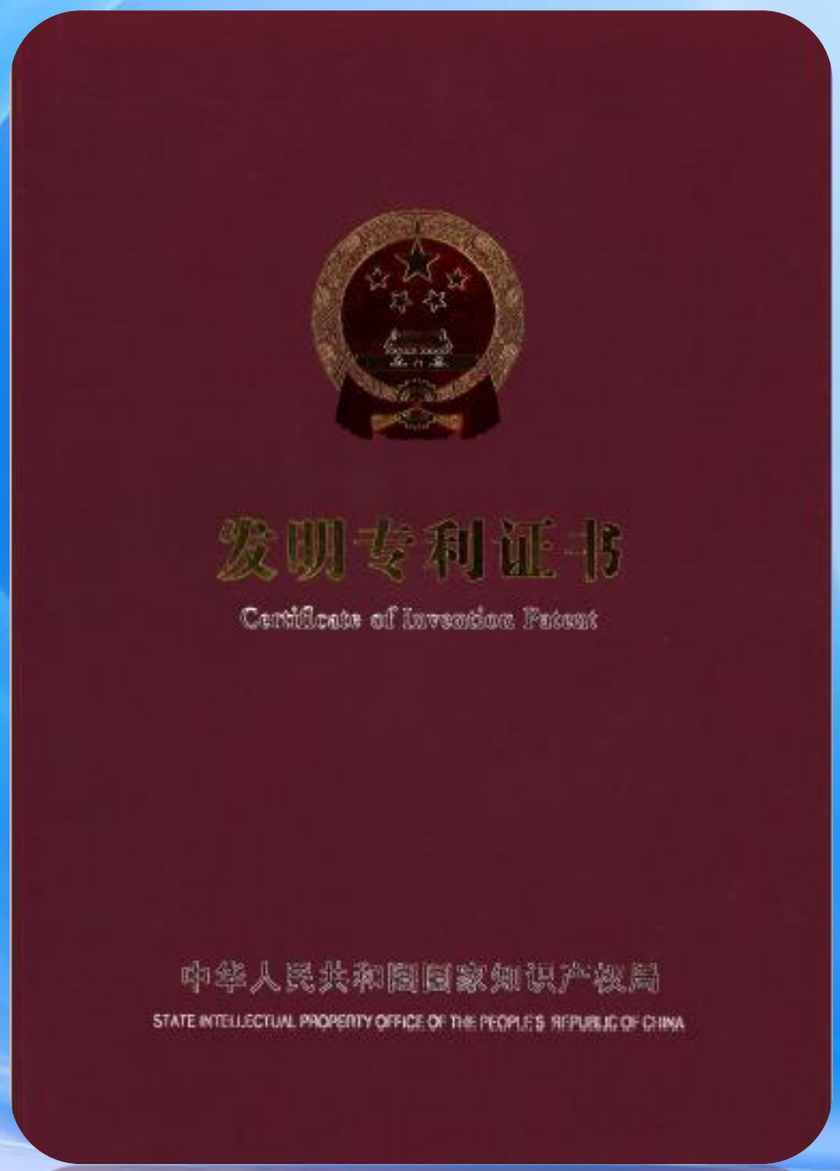
表：长龙主要专利内容描述及产业效果

Item	专利名称	概要描述	产业效果
2	Method f semiconc a substra	描述了在芯片焊盘表面形成绝缘层和导电体，通过隔离层中的接触腔和通孔连接芯片和基板焊点。此技术优化了芯片电气连接，提升了安装精度和可靠性，适合复杂电路封装。	为复杂电路封装提供早期电气连接解决方案，推动高精度、高可靠性封装的普及。
5	Semicond adapted f on a subs	提供一种通过微细互连技术将芯片焊盘与基板焊点连接的装置，增强了电气连接和结构可靠性，特别适用于多芯片模块封装，提高了封装的稳定性，并在早期阶段限制了竞争对手技术路线。	提升多芯片模块封装的稳定性，成为产业标准，降低竞争者在电气互连方面的技术发展空间。
9	Method f semiconc a substra	介绍了在芯片焊盘上形成导电凸块并涂覆光刻胶层的技术，通过在光刻胶层中形成通孔并填充金属材料实现稳定连接，提升了装配精度和电气性能，简化了传统封装流程。	优化装配精度并简化流程，为高密度和小尺寸芯片封装提供高效生产路径。
10	Method f semiconc a substra	使用多层导电结构提升芯片与基板的电气连接，在焊盘表面涂覆光刻胶层形成导电凸块，并通过通孔和多层互连结构增强电气连接，适用于高密度多芯片封装，优化了装配过程和性能。	支持高密度封装发展，促进多层互连技术的成熟和产业推广，适用于高性能芯片模块。

3D封装专利清单

項目	專利號	案弓名稱
1	US7383630	Method for making a circuit plate
2	US6774473	Semiconductor chip module
3	US6420788	Method for mounting a semiconductor chip on a substrate and semiconductor device adapted for mounting on a substrate
4	US6437448	Semiconductor device adapted for mounting on a substrate
5	US7176573	Semiconductor device with a multi-level interconnect structure and method for making the same
6	I241009	一種形成玄砲凸塊的方法及具布如此形成之電凸塊的裝置
7	I292178	堆疊式半導體晶片封裝體
8	US7411285	Low profile stacked semiconductor chip package
9	ZL200510117763.5	堆疊式半導體晶片封裝體
10	US8076775	Semiconductor package and method for making the same
11	US7672130	Heat dissipating device
12	ZL201110036515.3	散熱裝置

长龙国际与新马地区、大陆合肥地区合作3D封装相关项目




证书号第550086号

发明专利证书

发明名称：堆叠式半导体芯片封装体

发明人：沈育浓

专利号：ZL 2005 1 0117763.5

专利申请日：2005年11月10日

专利权人：沈育浓

授权公告日：2009年9月16日

本发明经过本局依照中华人民共和国专利法进行审查，决定授予专利权，颁发本证书并在专利登记簿上予以登记。专利权自授权公告之日起生效。

本专利的专利权期限为二十年，自申请日起算。专利权人应当依照专利法及其实施细则规定缴纳年费。缴纳本专利年费的期限是每年11月10日前一个月内。未按照规定缴纳年费的，专利权自应当缴纳年费期满之日起终止。

专利证书记载专利权登记时的法律状况。专利权的转移、质押、无效、终止、恢复和专利权人的姓名或名称、国籍、地址变更等事项记载在专利登记簿上。

局长 田力普

2009年9月16日

第1页(共1页)

The United States of America

The Director of the United States Patent and Trademark Office

Has received an application for a patent for a new and useful invention. The title and description of the invention are enclosed. The requirements of law have been complied with, and it has been determined that a patent on the invention shall be granted under the law.

Therefore, this

United States Patent

Grants to the person(s) having title to this patent the right to exclude others from making, using, offering for sale, or selling the invention throughout the United States of America or importing the invention into the United States of America, and if the invention is a process, of the right to exclude others from using, offering for sale or selling throughout the United States of America, or importing into the United States of America, products made by that process, for the term set forth in 35 U.S.C. 154(a)(2) or (c)(1), subject to the payment of maintenance fees as provided by 35 U.S.C. 41(b). See the Maintenance Fee Notice on the inside of the cover.

David J. Kappos

Director of the United States Patent and Trademark Office

US007411285B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 7,411,285 B2**
(45) **Date of Patent: Aug. 12, 2008**

(54) **LOW PROFILE STACKED SEMICONDUCTOR CHIP PACKAGE**

(76) Inventor: **Yu-Nung Shen**, No. 60, Lane 328, Li-Shan Street, Nei-Hu Dist., Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 250 days.

(21) Appl. No.: **11/302,210**

(22) Filed: **Dec. 14, 2005**

(65) **Prior Publication Data**

US 2007/0001294 A1 Jan. 4, 2007

(30) **Foreign Application Priority Data**

Jul. 1, 2005 (TW) ..... 94122920 A

(51) **Int. Cl.**
H01L 23/48 (2006.01)
H01L 23/02 (2006.01)

(52) **U.S. Cl.** **257/686**; 257/777; 257/778; 257/774; 257/E23.011

(58) **Field of Classification Search** 257/777, 257/686, 774, 778, E25.011, E21.614
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,577,013 B1 * 6/2003 Glenn et al. 257/777
6,774,475 B1 * 8/2004 Shen 257/686
6,858,926 B2 * 2/2005 Yamada et al. 257/774
7,276,799 B2 * 10/2007 Lee et al. 257/777
2004/0110362 A1 * 6/2004 Egawa 257/734
2004/0207949 A1 * 10/2004 Bauer et al. 257/620
2005/0093141 A1 * 1/2005 Hayasaka et al. 438/109

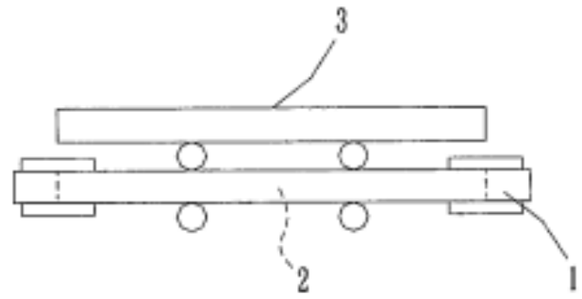
* cited by examiner

Primary Examiner—Nitin Parekh
(74) *Attorney, Agent, or Firm*—Houston Eliseeva LLP

(57) **ABSTRACT**

A stacked semiconductor chip package comprising a first semiconductor chip having an upper surface, a lower surface opposed to said upper surface, and a plurality of conductive metal lines formed on said upper surface of said first semiconductor chip, a plurality of metal elements each having a first area portion located on said upper surface of said first semiconductor chip and connected electrically to a corresponding one of said metal lines, a second area portion located on said lower surface of said first semiconductor chip, and a second semiconductor chip having a lower surface and a plurality of conductive bumps provided on said lower surface, and connected on said upper surface of said first semiconductor chip in such a manner that said solder bumps of said second semiconductor chip is electrically connected to said corresponding conductive metal lines on said upper surface of said first semiconductor chip.

8 Claims, 10 Drawing Sheets



US00807677582

(12) **United States Patent**
Shen

(10) **Patent No.: US 8,076,775 B2**
(45) **Date of Patent: Dec. 13, 2011**

(54) **SEMICONDUCTOR PACKAGE AND METHOD FOR MAKING THE SAME**

(76) Inventor: **Yu-Nung Shen**, Taipei (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 73 days.

(21) Appl. No.: **12/357,334**

(22) Filed: **Jan. 21, 2009**

(65) **Prior Publication Data**

US 2009/0194863 A1 Aug. 6, 2009

(30) **Foreign Application Priority Data**

Feb. 1, 2008 (TW) ..... 97104403 A

(51) **Int. Cl.**
H01L 23/04 (2006.01)

(52) **U.S. Cl.** . **257/730**; 257/686; 257/774; 257/E23.023; 257/E23.069; 257/E23.125; 438/106; 438/127; 361/777

(58) **Field of Classification Search** 257/686, 257/678, 690, 692, 693, 701, 730, 774, E23.061, 257/E25.023, E23.069, E23.125; 438/106, 438/109, 110, 125, 126, 127; 361/777
See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,888,884 A * 3/1999 Wojnarowski 438/462
7,045,899 B2 * 5/2006 Yamane et al. 257/777
7,112,469 B2 * 9/2006 Mihara 438/110
7,633,159 B2 * 12/2009 Boon et al. 257/730
7,790,505 B2 * 9/2010 Liu et al. 438/113
2001/0010627 A1 * 8/2001 Akagawa 361/761
2005/0051886 A1 * 3/2005 Mihara et al. 257/690
2005/0161799 A1 * 7/2005 Jobetto 257/690
2008/0237828 A1 * 10/2008 Yang 257/690

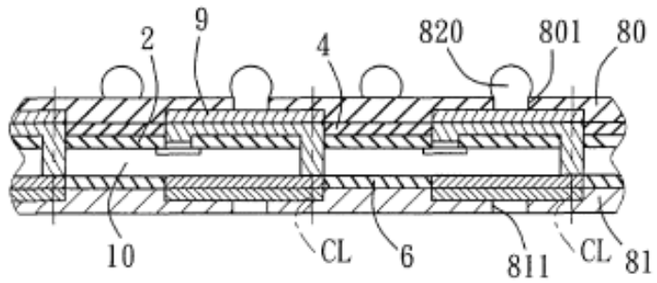
* cited by examiner

Primary Examiner — William D Coleman
Assistant Examiner — Su Kim
(74) *Attorney, Agent, or Firm* — Christie, Parker & Hale, LLP

(57) **ABSTRACT**

A semiconductor package includes: a semiconductor substrate; an inner insulator layer formed on the substrate; at least one internal wiring extending from a front side of the substrate along one of lateral sides of the substrate to a rear side of the substrate; a first outer insulator layer disposed at the front side of the substrate, formed on the internal wiring, and formed with at least one wire-connecting hole; and a second outer insulator layer disposed at the rear side of the substrate, formed on the internal wiring, and formed with at least one wire-connecting hole which exposes a portion of the internal wiring.

7 Claims, 8 Drawing Sheets



US006774473B1

(12) **United States Patent**
Shen

(10) **Patent No.: US 6,774,473 B1**
(45) **Date of Patent: Aug. 10, 2004**

(54) **SEMICONDUCTOR CHIP MODULE**

(75) Inventor: **Ming-Tung Shen**, 4F, No. 52, Sec. 2, Chung-Shan N. Rd., Taipei (TW)

(73) Assignee: **Ming-Tung Shen**, Taipei (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/407,284**

(22) Filed: **Sep. 28, 1999**

(30) **Foreign Application Priority Data**

Jul. 30, 1999 (TW) ..... 88212813 U

(51) **Int. Cl.**[7] **H01L 23/02**; H01L 23/34

(52) **U.S. Cl.** **257/686**; 257/778; 257/780; 257/723; 257/774; 257/782; 257/783

(58) **Field of Search** 257/686, 725, 257/738, 780, 782, 783, 778, 777, 774

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,731,633 A * 3/1998 Clayton 257/723
5,784,264 A * 7/1998 Tanioka 361/810
5,854,507 A * 12/1998 Miremadi et al. 257/686
5,977,640 A * 11/1999 Bertin et al. 257/777
6,025,648 A * 2/2000 Takahashi et al. 257/778
6,040,630 A * 3/2000 Fanchieu et al. 257/780
6,051,878 A * 4/2000 Akram et al. 257/686
6,089,793 A * 5/2000 Maruyama et al. 361/687
6,101,100 A * 8/2000 Leeds 361/761
6,137,164 A * 10/2000 Yew et al. 25/686
6,153,928 A * 11/2000 Cho 257/686
6,180,127 B1 * 2/2001 Sueba et al. 257/686
6,229,215 B1 * 5/2001 Egawa 257/777

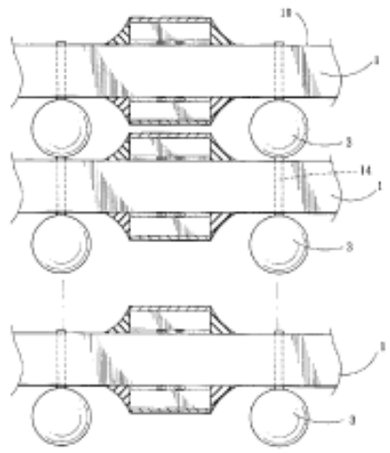
* cited by examiner

Primary Examiner—Steve Loke
Assistant Examiner—Nitin Parekh
(74) *Attorney, Agent, or Firm*—Merchant & Gould, P.C.

(57) **ABSTRACT**

A semiconductor chip module includes a chip-mounting member having opposite first and second surfaces, a set of circuit traces, and a plurality of plated through holes that extend through the first and second surfaces and that are connected to the circuit traces. A dielectric tape member bonds adhesively a semiconductor chip on the chip-mounting member. A first conductor unit connects electrically contact pads on a pad mounting surface of the semiconductor chip and the circuit traces. A plurality of solder balls are disposed on one of the first and second surfaces of the chip-mounting member, are aligned with and are connected to the plated through holes in the chip-mounting member, respectively.

8 Claims, 9 Drawing Sheets



US007176573B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 7,176,573 B2**
(45) **Date of Patent: Feb. 13, 2007**

(54) **SEMICONDUCTOR DEVICE WITH A MULTI-LEVEL INTERCONNECT STRUCTURE AND METHOD FOR MAKING THE SAME**

(76) Inventor: **Yu-Nung Shen**, 4F, No. 52, Sec. 2, Chang-Shan N. Rd., Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/716,948**

(22) Filed: **Nov. 19, 2003**

(65) **Prior Publication Data**

US 2004/0135257 A1 Jul. 15, 2004

(30) **Foreign Application Priority Data**

Nov. 22, 2002 (TW) ..... 91134054 A

(51) **Int. Cl.**
H01L 23/48 (2006.01)

(52) **U.S. Cl.** **257/758**

(58) **Field of Classification Search** 257/758, 257/734–738, 700; 438/118

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,175,158 B1 * 1/2001 Suzuki 257/778
6,713,859 B1 * 3/2004 Ma 257/687

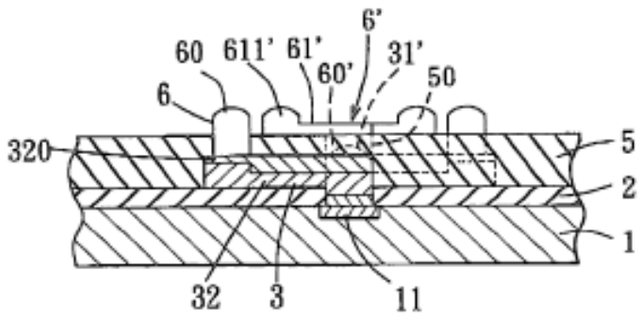
* cited by examiner

Primary Examiner—Nathan W. Ha

(57) **ABSTRACT**

A semiconductor device includes a semiconductor die and a multi-level interconnect structure that has a first insulating layer formed on the die, conductive horizontal bodies, each of which is connected to a respective bonding pad of the die and has an extension formed on the first insulating layer, a second insulating layer formed on the first insulating layer, and conductive vertical bodies, each of which is connected to the extension of a respective conductive horizontal body and extends through the second insulating layer.

20 Claims, 4 Drawing Sheets



US007383630B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 7,383,630 B2**
(45) **Date of Patent: Jun. 10, 2008**

(54) **METHOD FOR MAKING A CIRCUIT PLATE**

(76) Inventor: **Yu-Nung Shen**, 4F, No. 52, Sec. 2, Chang-Shan N. Rd., Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 312 days.

(21) Appl. No.: **11/166,058**

(22) Filed: **Jun. 24, 2005**

(65) **Prior Publication Data**

US 2006/0000635 A1 Jan. 5, 2006

(30) **Foreign Application Priority Data**

Jun. 30, 2004 (TW) ..... 93119684 A

(51) **Int. Cl.**
H01K 3/10 (2006.01)
H05K 3/02 (2006.01)

(52) **U.S. Cl.** **29/852**; 29/835; 29/846; 29/847; 29/848

(58) **Field of Classification Search** 29/835, 29/846, 847, 848, 852

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,678,952 B2 * 1/2004 Juntl 29/847
7,174,638 B2 * 2/2007 Hsu et al. 29/842
2001/0040298 A1 * 11/2001 Sakassi et al. 257/737

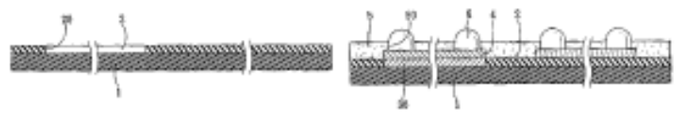
* cited by examiner

Primary Examiner—C. J Arbes
(74) *Attorney, Agent, or Firm*—Ladas and Parry LLP

(57) **ABSTRACT**

A method for making a circuit plate includes: forming first holes in an insulating layer; forming a conductive layer on the insulating layer such that a portion of the conductive layer fills the first holes; grinding the conductive layer such that the portion of the conductive layer remains in the first holes to form a pattern of conductive traces; forming a dielectric protective layer that covers the insulating layer and the conductive traces; forming a pattern of second holes in the protective layer such that a portion of each of the conductive traces is accessible through a respective one of the second holes; and forming conductive bumps that are respectively connected to the conductive traces.

14 Claims, 5 Drawing Sheets



US007383630B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 7,383,630 B2**
(45) **Date of Patent: Jun. 10, 2008**

(54) **METHOD FOR MAKING A CIRCUIT PLATE**

(76) Inventor: **Yu-Nung Shen**, 4F, No. 52, Sec. 2, Chung-Shan N. Rd., Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 312 days.

(21) Appl. No.: **11/166,058**

(22) Filed: **Jun. 24, 2005**

(65) **Prior Publication Data**

US 2006/0000635 A1 Jan. 5, 2006

(30) **Foreign Application Priority Data**

Jun. 30, 2004 (TW) ..... 93119684 A

(51) **Int. Cl.**
H01K 3/10 (2006.01)
H05K 3/02 (2006.01)

(52) **U.S. Cl.** **29/852**; 29/835; 29/846; 29/847; 29/848

(58) **Field of Classification Search** 29/835, 29/846, 847, 848, 852

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,678,952 B2 * 1/2004 Jamil 29/847
7,174,638 B2 * 2/2007 Hsu et al. 29/842
2001/0040298 A1 * 11/2001 Sakurai et al. 257/737

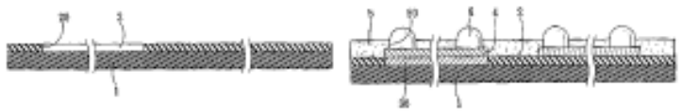
* cited by examiner

Primary Examiner—C. J Arbes
(74) *Attorney, Agent, or Firm*—Ladas and Parry LLP

(57) **ABSTRACT**

A method for making a circuit plate includes: forming first holes in an insulating layer; forming a conductive layer on the insulating layer such that a portion of the conductive layer fills the first holes; grinding the conductive layer such that the portion of the conductive layer remains in the first holes to form a pattern of conductive traces; forming a dielectric protective layer that covers the insulating layer and the conductive traces; forming a pattern of second holes in the protective layer such that a portion of each of the conductive traces is accessible through a respective one of the second holes; and forming conductive bumps that are respectively connected to the conductive traces.

14 Claims, 5 Drawing Sheets



US006437448B1

(12) **United States Patent**
Chen

(10) **Patent No.: US 6,437,448 B1**
(45) **Date of Patent: Aug. 20, 2002**

(54) **SEMICONDUCTOR DEVICE ADAPTED FOR MOUNTING ON A SUBSTRATE**

(76) Inventor: **I-Ming Chen**, No. 60, Lane 328, Li-Shan St., Nei-Hu Dist., Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/765,793**

(22) Filed: **Jan. 18, 2001**

Related U.S. Application Data

(63) Continuation-in-part of application No. 09/725,431, filed on Nov. 29, 2000.

(30) **Foreign Application Priority Data**

Oct. 21, 2000 (TW) ..... 89108578 A

(51) **Int. Cl.**[7] **H01L 23/48**; H01L 23/52; H01L 29/40

(52) **U.S. Cl.** **257/777**; 257/737

(58) **Field of Search** 257/737, 738, 257/777, 778, 779, 780, 781, 782, 784, 787

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,222,014 A * 6/1993 Lin 361/414
5,990,546 A * 11/1999 Igasaki et al. 257/700
6,143,991 A * 11/2000 Moriyama 174/261
6,200,143 B1 * 3/2001 Haba et al. 439/70
6,239,488 B1 * 5/2001 Chen 257/737

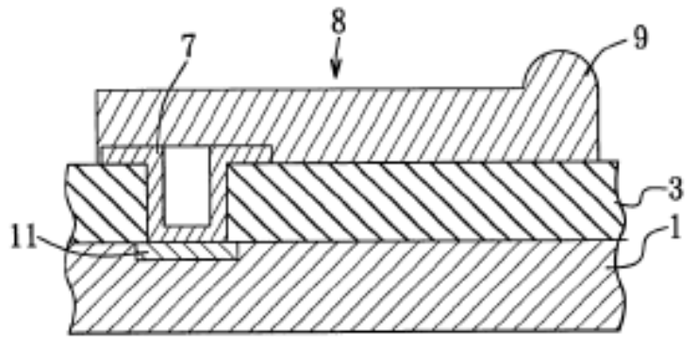
* cited by examiner

Primary Examiner—Viet Q. Nguyen
Assistant Examiner—Ehsan Nhu
(74) *Attorney, Agent, or Firm*—Christensen O'Connor; Johnson Kindness PLLC

(57) **ABSTRACT**

A method for manufacturing a semiconductor device includes the steps of providing a semiconductor chip having a pad-mounting surface with a bonding pad, forming a first bump on the bonding pad, forming a photoresist layer on the pad-mounting surface, forming a second bump which protrudes from the first bump through an upper surface of the photoresist layer, and forming a conductive body on the second bump. The conductive body has an anchor portion connecting electrically with and encapsulating an upper portion of the second bump, and a contact portion offset from the anchor portion and adapted to be connected to a substrate.

11 Claims, 4 Drawing Sheets




US007672130B2

(12) **United States Patent**
Shen

(10) **Patent No.: US 7,672,130 B2**
(45) **Date of Patent: Mar. 2, 2010**

(54) **HEAT DISSIPATING DEVICE**

(76) Inventor: **Yu-Nung Shen**, No. 60, Lane 328 Li-Shan Street, Nei-Hu District, Taipei City (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **12/229,971**

(22) Filed: **Aug. 27, 2008**

(65) **Prior Publication Data**

US 2009/0059527 A1 Mar. 5, 2009

(30) **Foreign Application Priority Data**

Aug. 31, 2007 (TW) ..... 96214647 U

(51) **Int. Cl.**
H05K 7/20 (2006.01)

(52) **U.S. Cl.** **361/699**; 361/700; 165/104.21; 165/148; 165/165; 422/129

(58) **Field of Classification Search** 361/695, 361/699, 700, 704

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,910,528 B2 * 6/2005 Ahiko et al. 165/168
7,017,657 B2 * 3/2006 Sagito et al. 165/104.21
7,272,009 B2 * 9/2007 Campbell et al. 361/699
2006/0096746 A1 * 5/2006 Agata et al. 165/166
2006/0165570 A1 * 7/2006 Knopf et al. 422/224

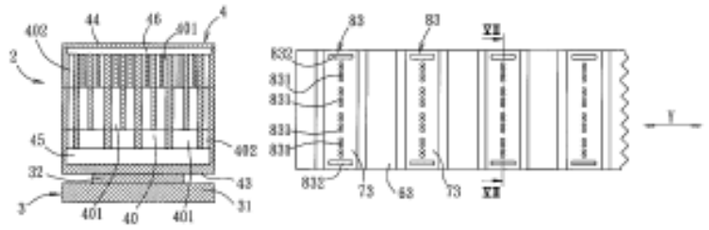
* cited by examiner

Primary Examiner—Jayprakash N Gandhi
Assistant Examiner—Courtney Smith
(74) *Attorney, Agent, or Firm*—Townsend and Townsend and Crew, LLP

(57) **ABSTRACT**

A heat dissipating device includes a sealed container having hollow floors and floor-spacing assemblies. Each floor-spacing assembly includes hollow spacing walls. Each hollow spacing wall extends from a respective hollow floor and is spaced apart from an adjacent one of the hollow spacing walls of an adjacent one of the floor-spacing assemblies by an air gap. Each two adjacent ones of the hollow floors are interconnected through the hollow spacing walls disposed therebetween. The sealed container defines a liquid reservoir, a condensate reservoir, and a plurality of fluid passages extending through the hollow spacing walls and the hollow floors that are disposed between the liquid reservoir and the condensate reservoir.

9 Claims, 6 Drawing Sheets



全球半导体和内存市场

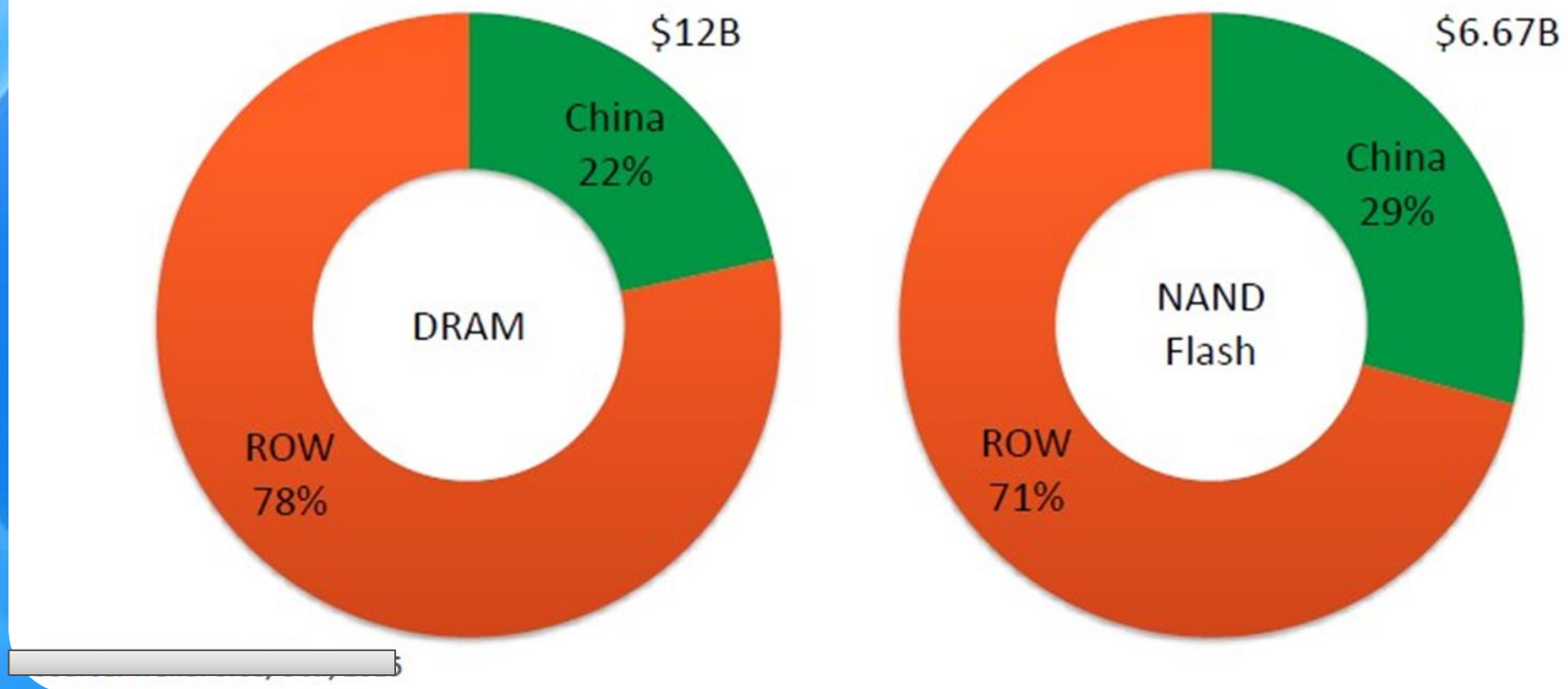
内存占全球半导体四分之一的产量

数据存取需求爆炸性的成长

1 ZB = 10^{21} bytes = 1000,000,000,000 GB

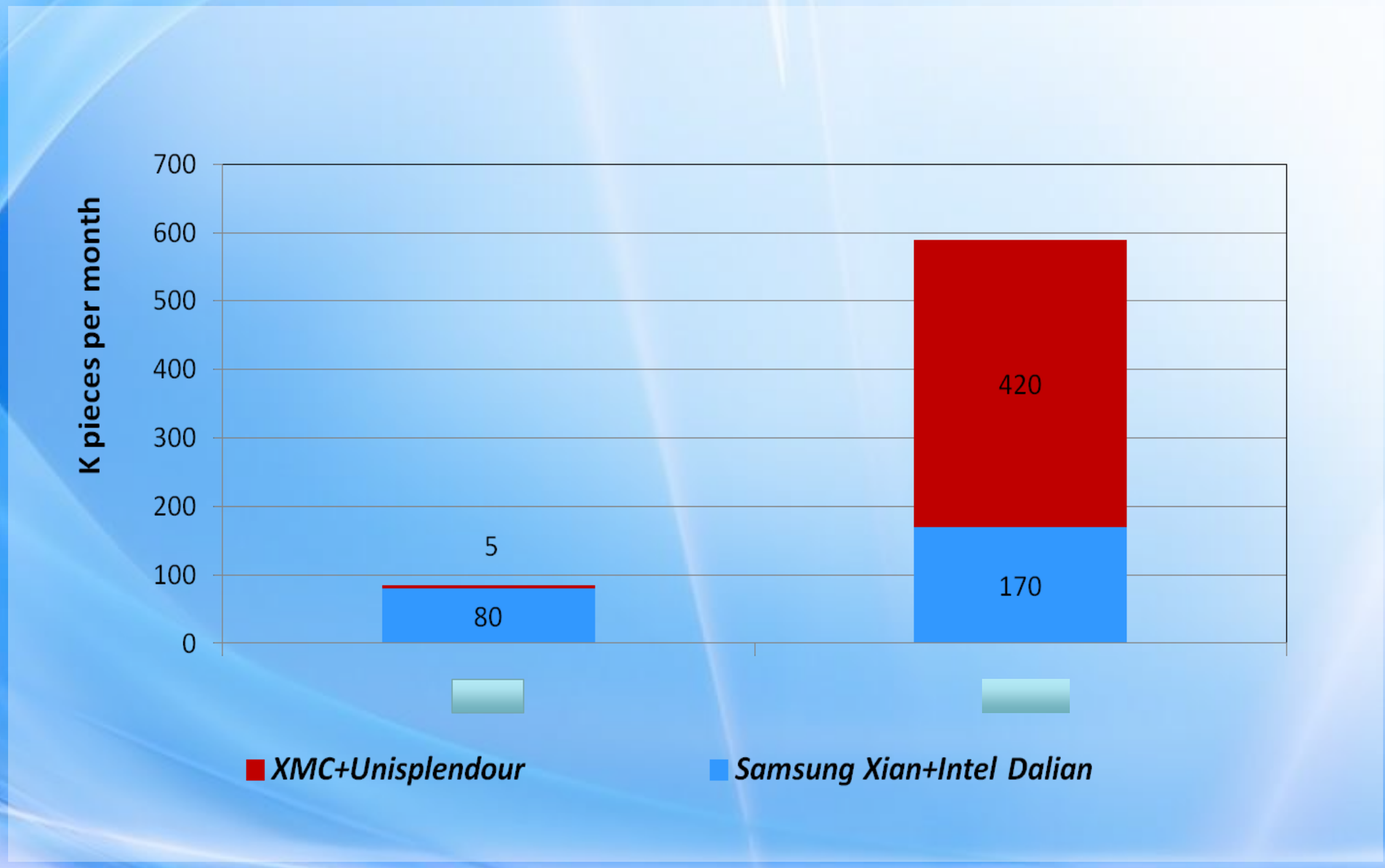
大数据显示“移动/计算应用中的广泛部署而正在创建。
数据是未来十年的新“石油”。

中国的内存需求

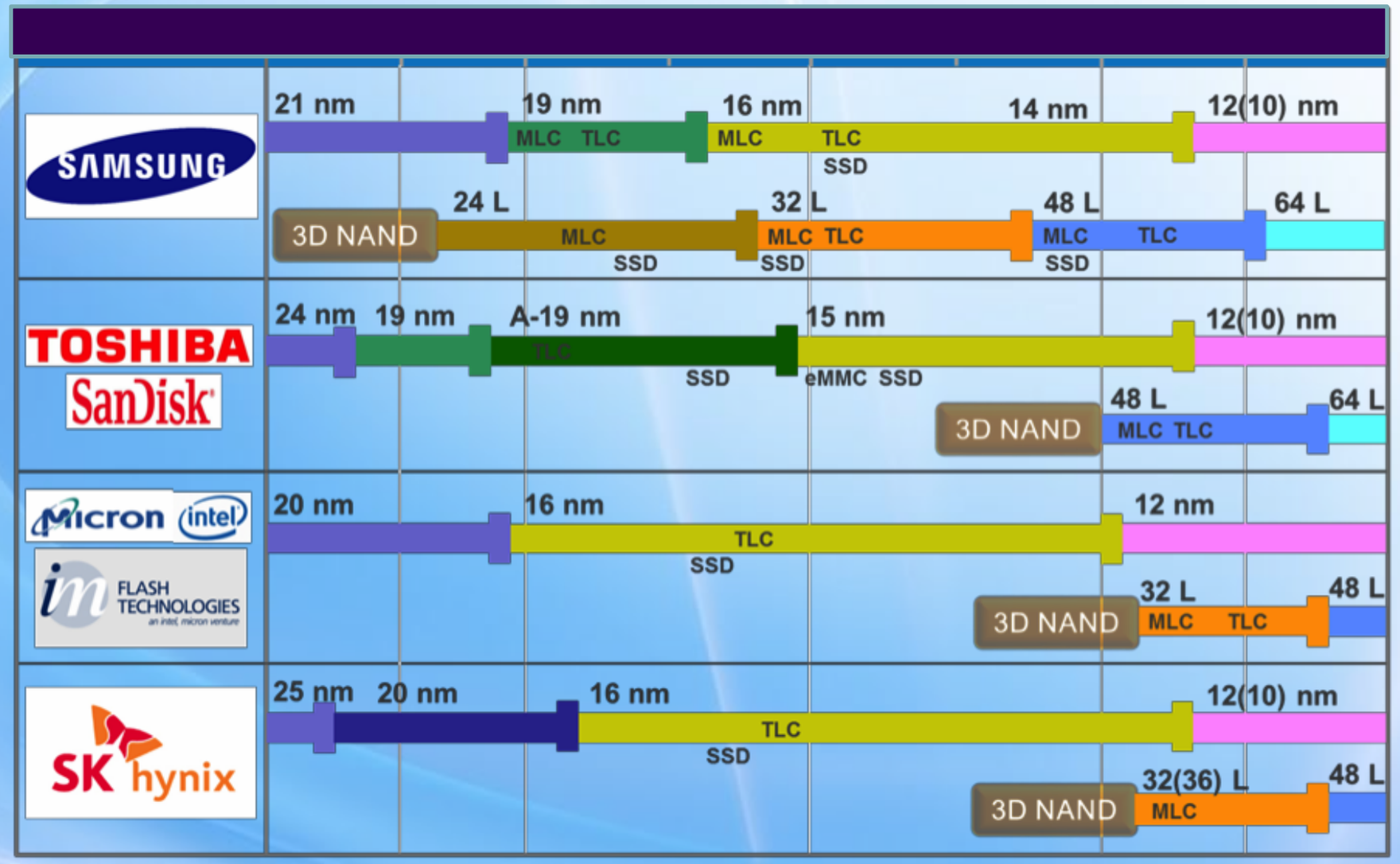


隨著PC智能手機的興起，中國國內DRAM和NAND閃存消費量急劇增加。 中國占世界記憶產量的30%左右，其中大部分都是由國外進口製造。

NAND Flash需求



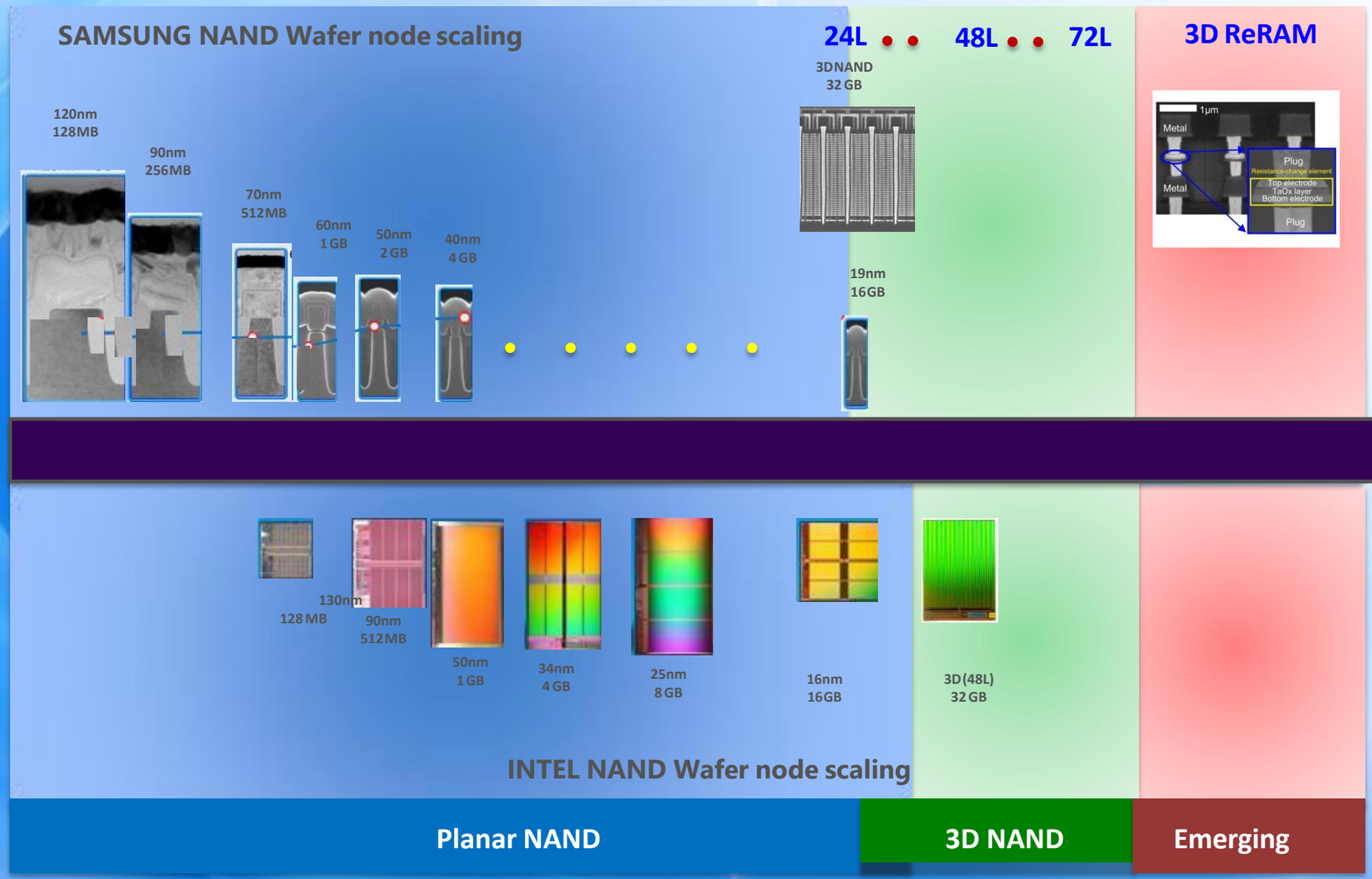
各厂3D封装技术进程


SAMSUNG
21 nm
19 nm
16 nm
14 nm
12(10) nm
MLC TLC
MLC TLC
SSD
3D NAND
24 L
32 L
48 L
64 L
MLC
MLC TLC
MLC TLC
SSD
SSD
SSD
TOSHIBA
SanDisk
24 nm
19 nm
A-19 nm
15 nm
12(10) nm
TLC
SSD
eMMC SSD
3D NAND
48 L
64 L
MLC TLC
Micron
intel
FLASH TECHNOLOGIES
20 nm
16 nm
12 nm
TLC
SSD
3D NAND
32 L
48 L
MLC
TLC
SK hynix
25 nm
20 nm
16 nm
12(10) nm
TLC
SSD
3D NAND
32(36) L
48 L
MLC

全球半导体中心的战略图

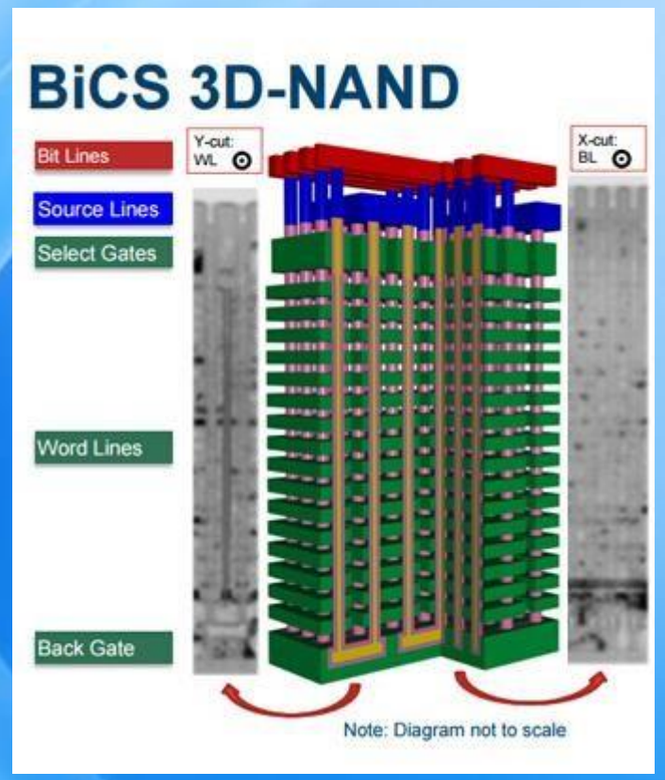
Zoom in on China factory locations

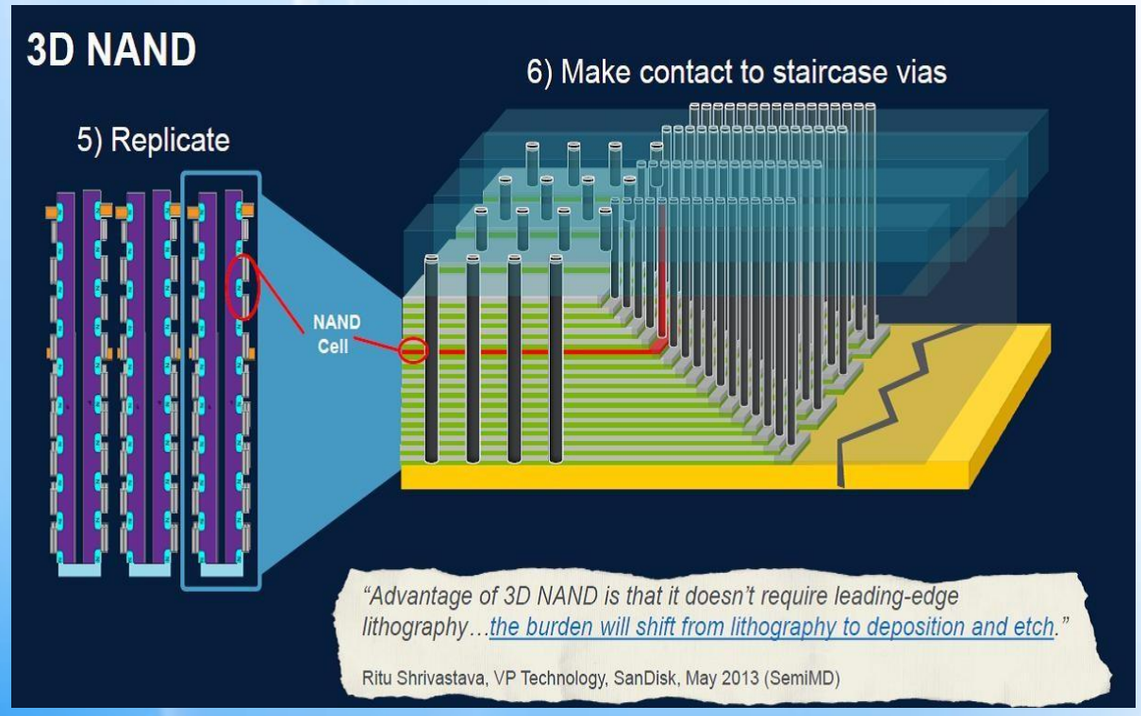
3D NAND发展进程

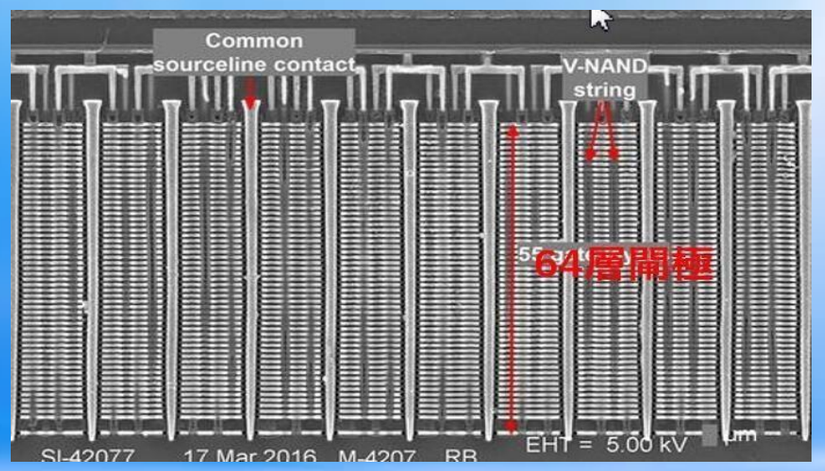


3D NAND技术提供的扩展经济效益显著降低了

3D封装技术概念图


BiCS 3D-NAND
Bit Lines
Source Lines
Select Gates
Word Lines
Back Gate
Y-cut: WL
X-cut: BL
Note: Diagram not to scale


3D NAND
5) Replicate
6) Make contact to staircase vias
NAND Cell
"Advantage of 3D NAND is that it doesn't require leading-edge lithography…the burden will shift from lithography to deposition and etch."
Ritu Shrivastava, VP Technology, SanDisk, May 2013 (SemiMD)


Common sourceline contact
V-NAND string
64層開極
EHT = 5.00 kV

3D封装技术应用范围


SSD
Solid State Drive
512GB
SATA 6Gb/s
9:12
acer
16:26
04:30
128GB

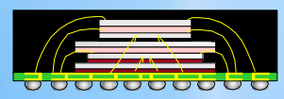
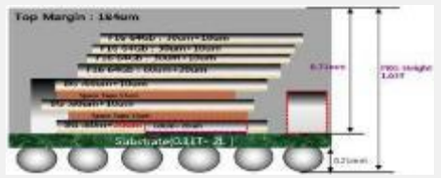
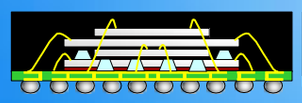
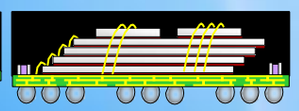
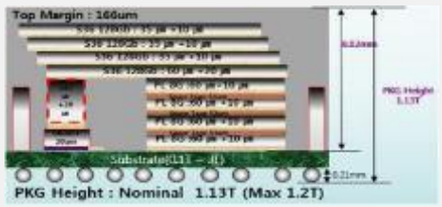
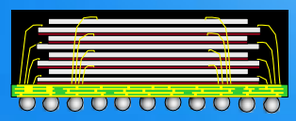
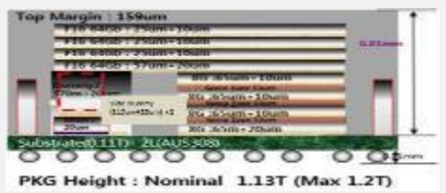
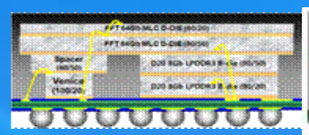
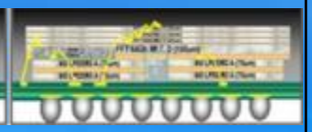
各种堆栈方式应用范围

REMOVABLE	MOBILE / WEARABLE	CLIENT SSD	ENTERPRISE SSD	AUTOMOTIVE
TSOP	Single chip eWLB	FLIP CHIP (SSD Controller)	FBGA-SD	SD -SiP
SD -SiP	UFS	FBGA-SD		TSOP
USB-SiP	eMMC			MicroSD
MicroSD	eMCP			

记忆替封装趋势

目前技术 → 趋势

HVM

PoP	FBGA	LGA	
FBGA-PoPt-SD2(2D) 	FBGA-SD4(4D+3W)  FBGA-SD5(5D+2W) 	Micro SD 4+1 SD SiP 	 TFBGA-SD7, 30 um WT, 1.03mm PGK T
FBGA-PoPt-SD3(3D+2W) 	FBGA-SD4(4D+0W)  FBGA-SD6, eMMC 	Dual Driver USB 8+1 	 TFBGA-SD8, 35 um WT, 1.13mm PGK T
FBGA-PoPt-SD4(4D+1W) 	FBGA-SD8(8D+0W)  VFBGA-SiP-SD8 	SD-SiP 	 TFBGA-SD8, 25 um WT, 1.13mm PGK T
FBGA-PoPt-SD4 	VFBGA-MD6  VFBGA-MD7 		
WFBGA-PoPt-SD4 	VFBGA-SiP-SD8  VFBGA-SiP-SD9 		 XL/MC-eWLB

L=1.4mm, T=1.2mm, V=1.0mm, W=0.8mm, U=0.65mm, X=0.50mm

LFBGA-SD8 (NAND)

Package Features

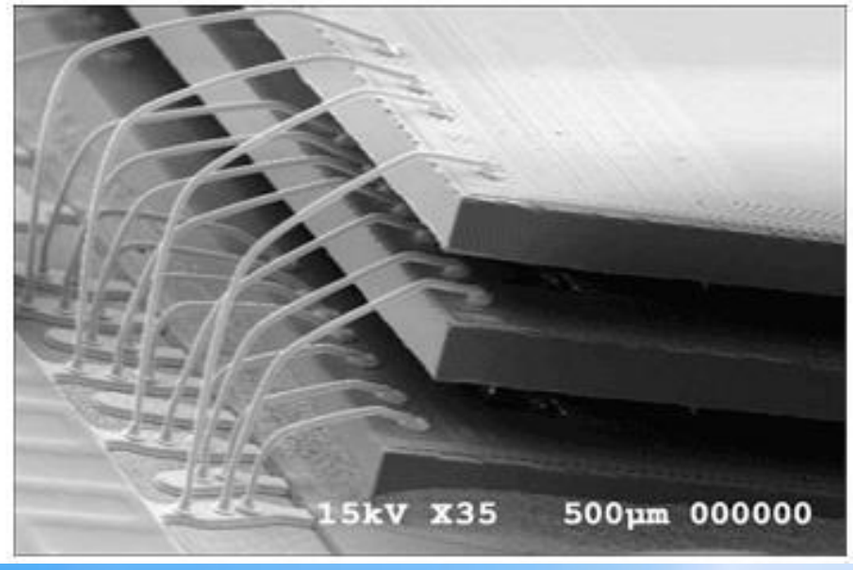
- LFBGA 14x18mm 152LD
- NAND Die Size : 9.7x17.1mm
- Device : 20nm Non-LowK NAND
- Wafer thickness : 60um
- Mold cap: 0.84mm
- 2-lyr / 0.13mmT laminate substrate

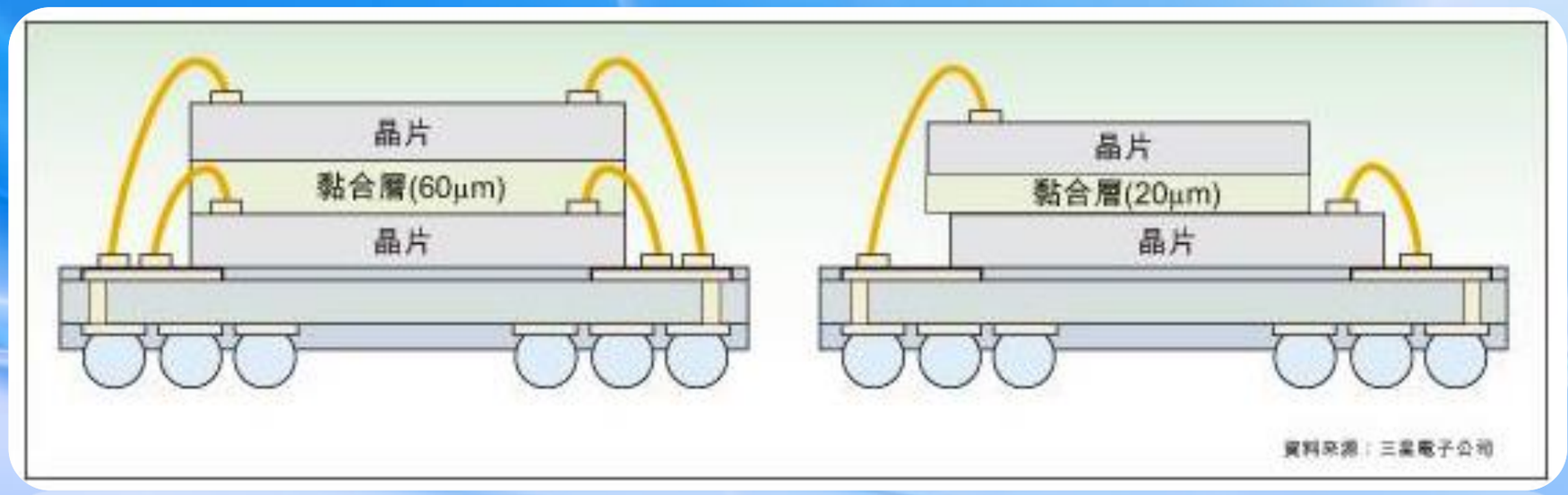
Key Technologies

- 20nm NAND die
- 0.5mm overhang W/B with 60um die thickness
- 2-passes DA for the 8 dies stack

Current Status

- **HVM since 2024**





内存堆栈芯片封装– MIXED (FBGA-SD6)
NAND + DDR + CONTROLLER

Package Features

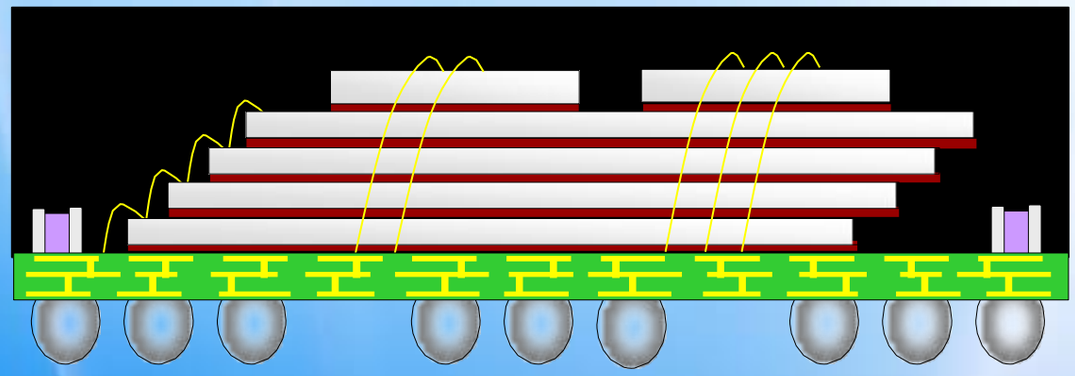
- VFBGA-SD6 11.5x13mm 153LD
- Nand flash Die Size: 10.33x8.12mm
- DDR Die Size: 6.32x2.69mm
- Controller Die Size: 6.79X1.82mm
- 0.13mm, 3-lyr coreless substrate

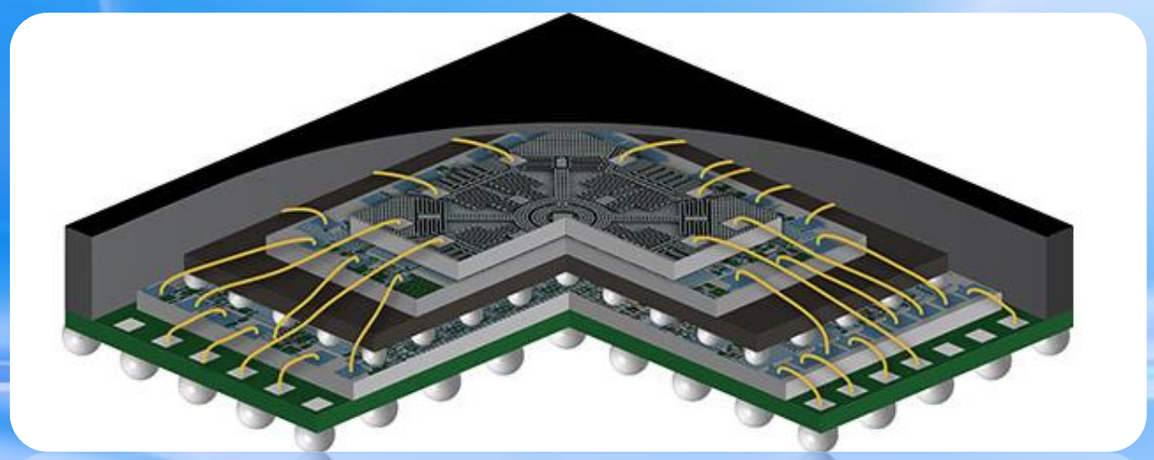
Key Technologies

- 0.13T odd layer substrate handing
- SSB loop for die to die and die to substrate
- Warpage control w/ 3L substrate

Current Status

- **HVM since 2024**





FLGA-SD9 (USB)

Package Features

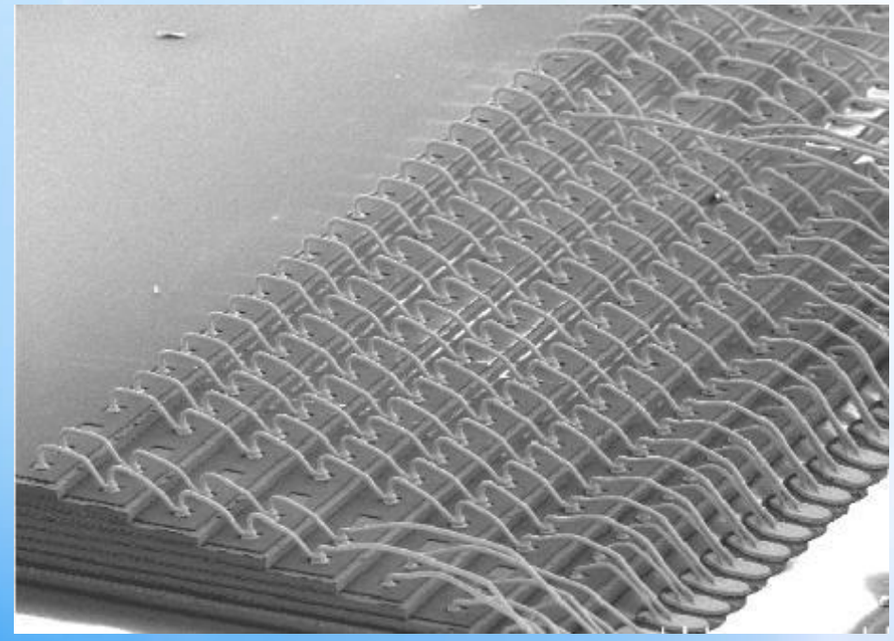
- FLGA 11.1x16mm
- Memory Die Size : 8.2x11.1mm
- Controller Die Size: 2.9x2.4mm
- Device : 19nm Non-LowK + 65nm Lowk Controller
- Wafer thickness : 68um x 8 dies + 150um Controller
- 2-lyr / 0.21mmT laminate substrate

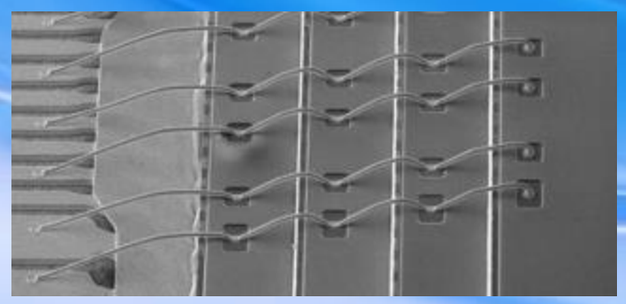
Key Technologies

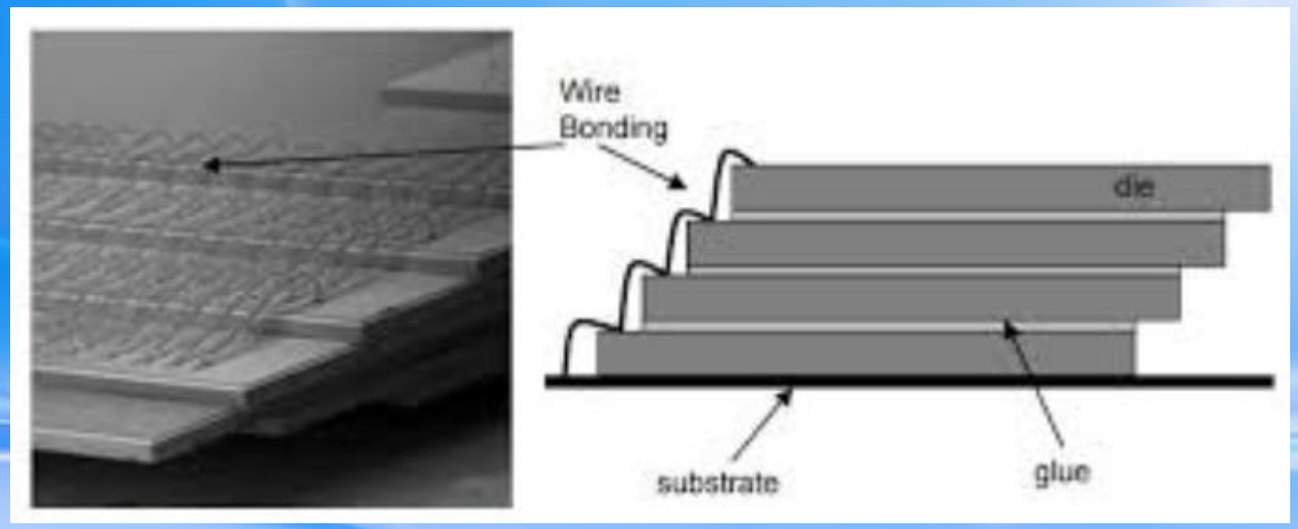
- 19nm NAND die
- 8-Die Stack with Die-to-die bonding
- One-pass for the 8 NAND dies stack

Current Status

- **HVM**







Memory Stacked-Die

Package Features

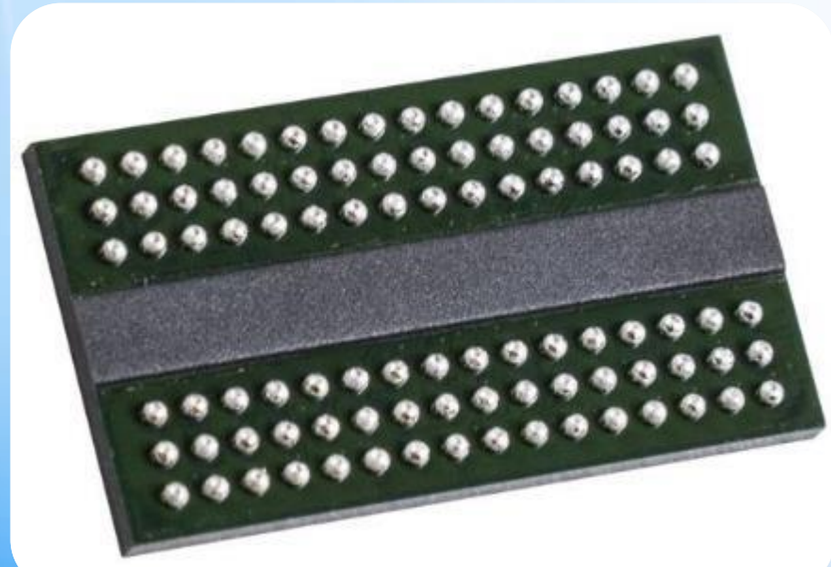
- FBGA 11.5x13mm 221LD e-MCP
- 4.115x1.385(Controller) : 60um
- 9.647x8.070(DRAM) : 75um
- 1.208x7.171(Nand) : 60um
- 9.00x8.00 (Film spacer) : 53um
- 2-lyr / 0.41mmT laminate substrate

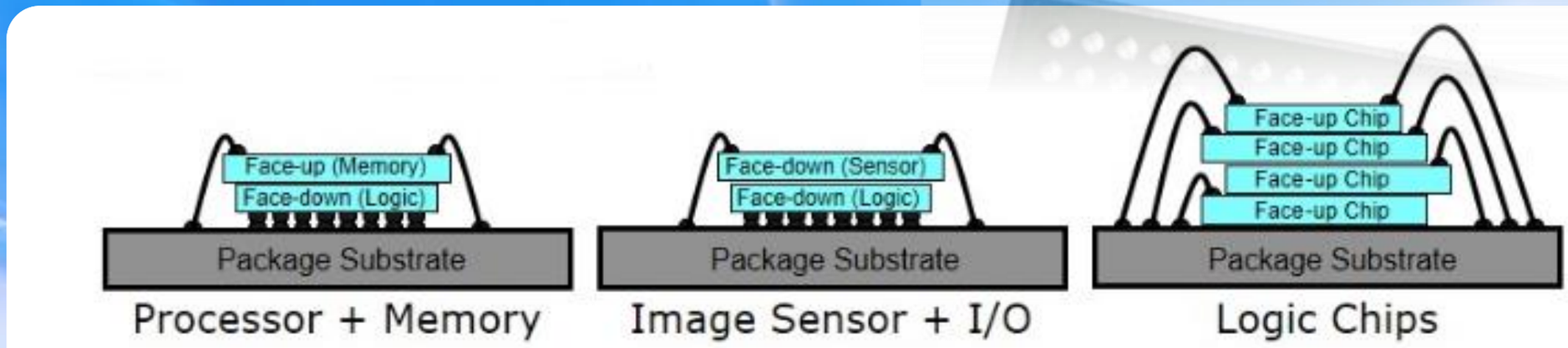
Key Technologies

- 60um NAND flash die
- Film spacer application
- Dolmen and NAND cascade structure

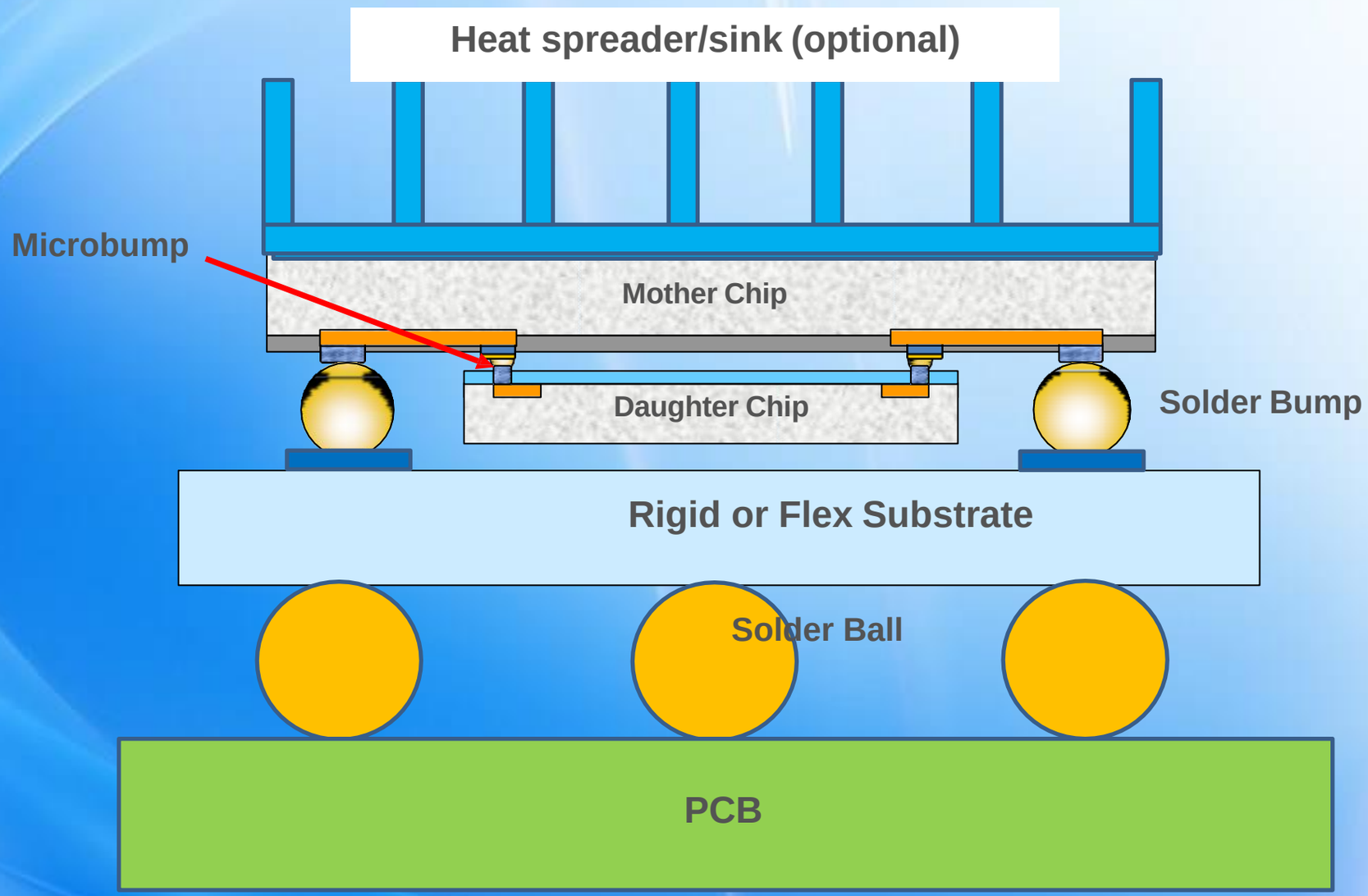
Current Status

- **HVM from ‘2024**



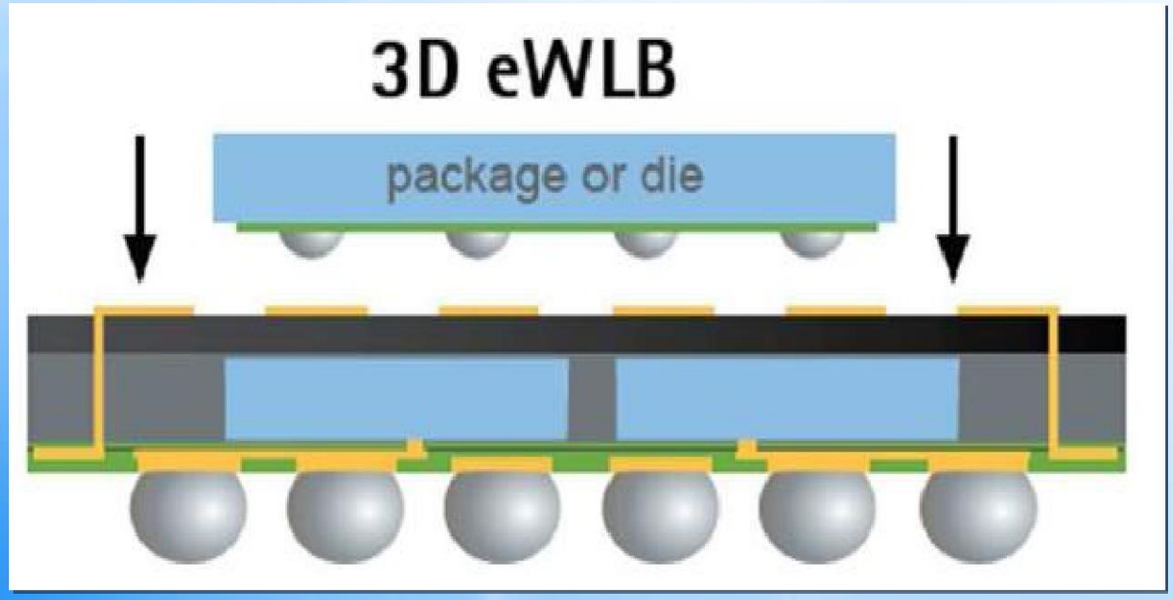


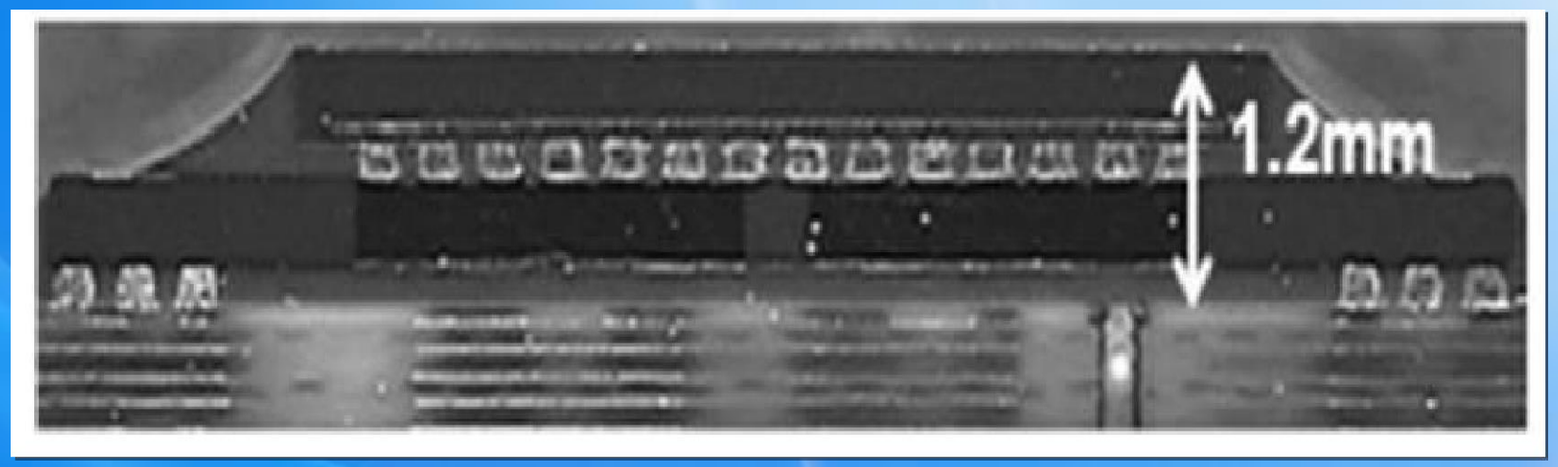
堆栈硅模块连接在基板上



Chip-to-Chip and Face-to-Face

半导体3D堆栈方式



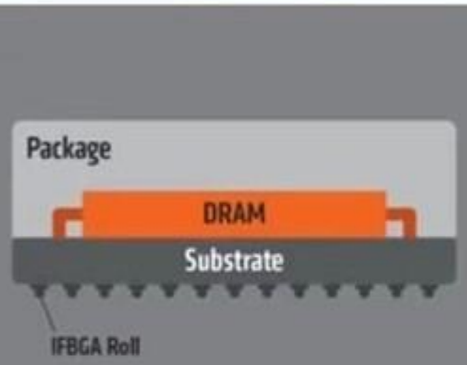


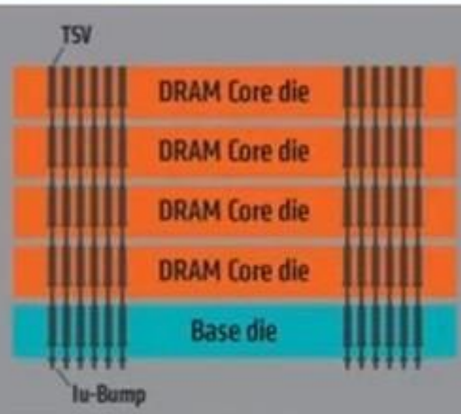
❒ 高頻寬記憶體(HBM)相關供應鏈

	SK海力士	三星	美光
準備量產	2024 Q4	2024 Q3	2024 Q4
DRAM製程	1β（1-beta）	1α（1-alpha）	1β（1-beta）
堆疊層數	12層	12層	12層

資料來源：https://uanalyze.com.tw/articles/892755582。

❒ 動能隨機存取記憶體(DRAM)的差異

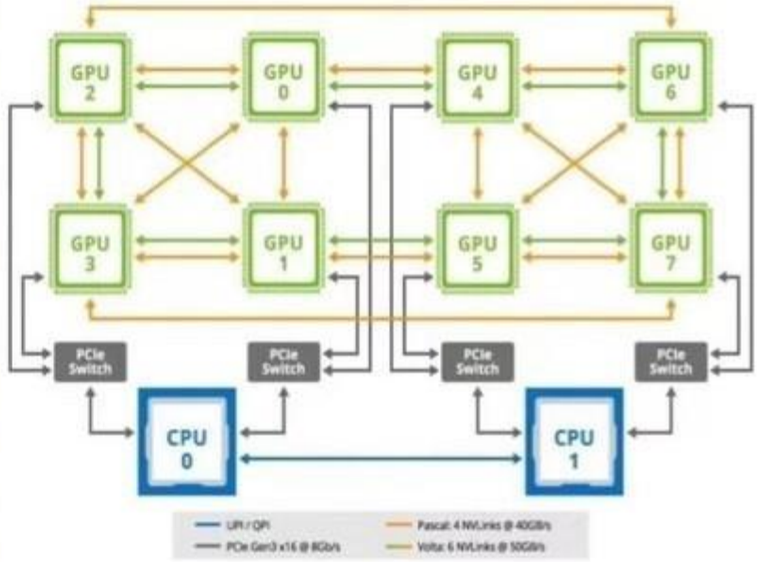




GDDR5	Per Package	HBM
32-bit	Bus Width	1024-bit
Up to 1750MHz (7GBps)	Clock Speed	Up to 500MHz (1GBps)
Up to 28GB/s per chip	Bandwidth	>100GB/s per stack
1.5V	Voltage	1.3V

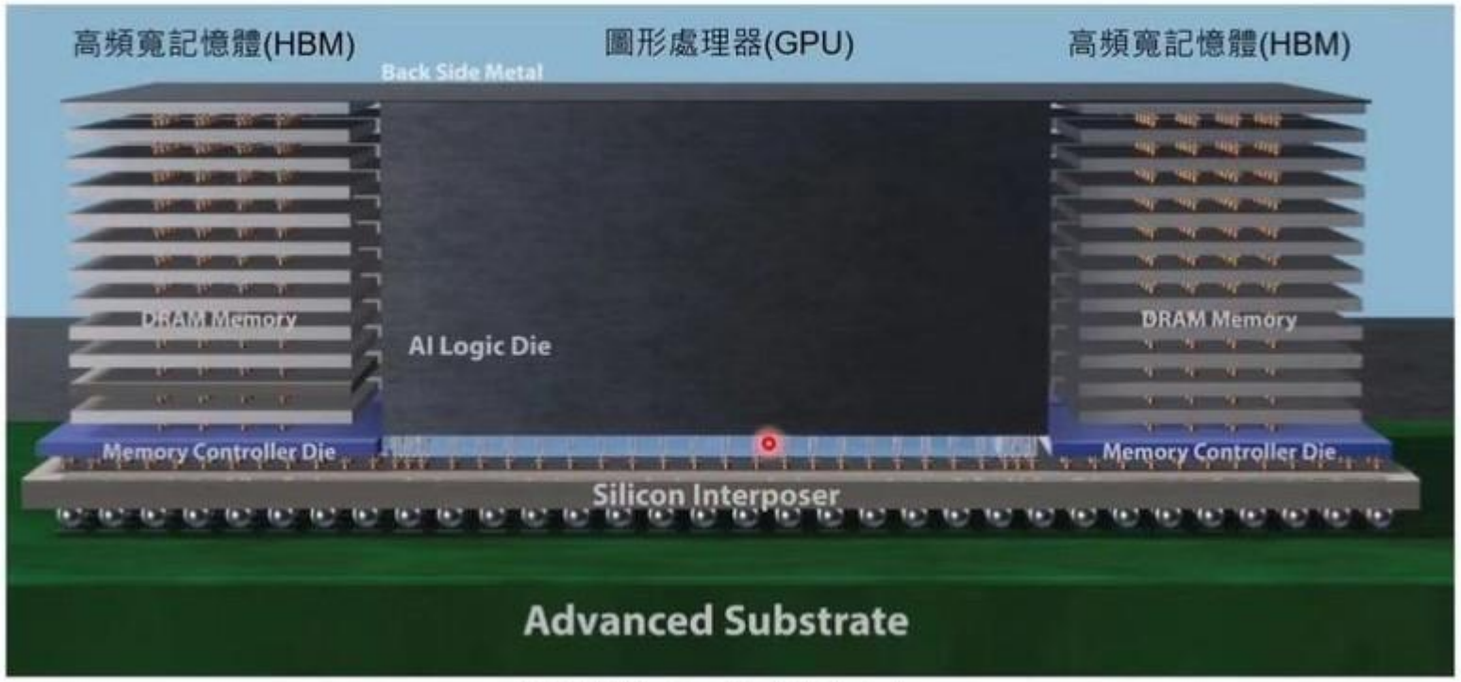
資料來源：AMD。

❒ NVIDIA Tesla P100 8x SXM2 GPU system



資料來源：https://www.servethehome.com/nvidia-dgx-versus-nvidia-hgx-what-is-the-difference/。

❒ 圖形處理器(GPU)與高頻寬記憶體(HBM)



資料來源：Applied Materials。

THANK YOU!